USB97C202

USB2.0 ATA/ ATAPI Controller

Datasheet

Product Features

- 2.5 Volt, Low Power Core Operation
- 3.3 Volt I/O with 5V input tolerance
- Complete USB Specification 2.0 Compatibility
  - Includes USB2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- Complete System Solution for interfacing ATA or ATAPI devices to USB2.0 bus
  - Supports USB Mass Storage Compliant Bootable BIOS
  - Supports ATA6 Drive capacities up to 2048GB
  - True UDMA Mode 4 transfer rates
  - Support for ATAPI Devices:
    - CD-ROM
    - CD-R
    - CD-RW
    - DVD
    - DVD/R/W
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal or External Program Memory Interface
  - 48K Byte Internal ROM or optional 64K Byte External Code Space using Flash, SRAM, or EPROM Memory
- On Board 12Mhz Crystal Driver Circuit
- Internal PLL for 480Mhz USB2.0 Sampling, 30Mhz MCU clock, and 60Mhz ATA clock
- Supports firmware upgrade via USB bus if “boot block” Flash program memory is used for optional external program memory
- 7 GPIOs for special function use: LED indicators, button inputs, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
  - USB High Speed LED
  - Serial EEPROM interface for VID/PID/Serial Number Customization (Required for internal ROM operation)
- Can share drive in MP3 player and 1394/USB applications by isolating the IDE Interface with other controllers.
- 100 Pin STQFP (12x12x1.4 body, 2mm footprint) or 100 Pin TQFP (14x14x1.4 body, 2mm footprint) package.

ORDERING INFORMATION

Order Number(s):

USB97C202-MN-04 for 100 pin STQFP package

USB97C202-MN-05 for 100 pin STQFP package

USB97C202-MD-05 for 100 pin TQFP package

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USB97C202 Datasheet Revision History

NAME	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
H. Wurzburg	Features	Modified third sub bullet under 7 GPIO's	Rev 1.6 (11-05-04)
M.Bohm	Ordering Information, cover	Changed the firmware extension from -04 to -05 for the order numbers	Rev 1.6 (9-29-04)
M.Bohm	Chapter 9 Package Outline, page 19	Added the 100 pin TQFP package	Rev 1.6 (9-29-04)
P. Konasewich	References to TQFP package changed to STQFP package.		Rev. 1.5 (02-04-04)
M. Bohm	Cover – Ordering Information	Removed USB97C202-MN-03.	Rev. 1.5 (11-07-03)
M. Bohm	Table 7.1 - DC Electrical Characteristics, page 15	Revised Input Leakage.	Rev. 1.5 (11-04-03)
M. Bohm	Chapter 2 - Pin Table, page 6	Changed test pin names to nTEST0, nTEST1 & nTEST2	Rev. 1.5 (11-04-03)
M. Bohm	Table 5.1 - USB97C202 Pin Descriptions, page 9	Changed nTest[0:2] to nTEST[0:2] and clarified the functionality of the XNOR test function.	Rev. 1.5 (11-04-03)
H. Wurzburg	Table 5.1 - USB97C202 Pin Descriptions, page 9	Revised description of the following pins: GPIO1 and GPIO4.	Rev. 1.4 (04/02/03)
	Ordering information, Cover	Added order numbers USB97C202-MN-03 and USB97C202-MN-04	1/23/03
	Features, Cover	Added feature bullet: Can share drive in MP3 player and 1394/USB applications by isolating the IDE Interface with other controllers.	1/09/03
	Table 5.1 - USB97C202 Pin Descriptions, page 9	Added the following description: In part number USB97C202-MN-03 or later ROM codes.	1/09/03

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Chapter 1 General Description

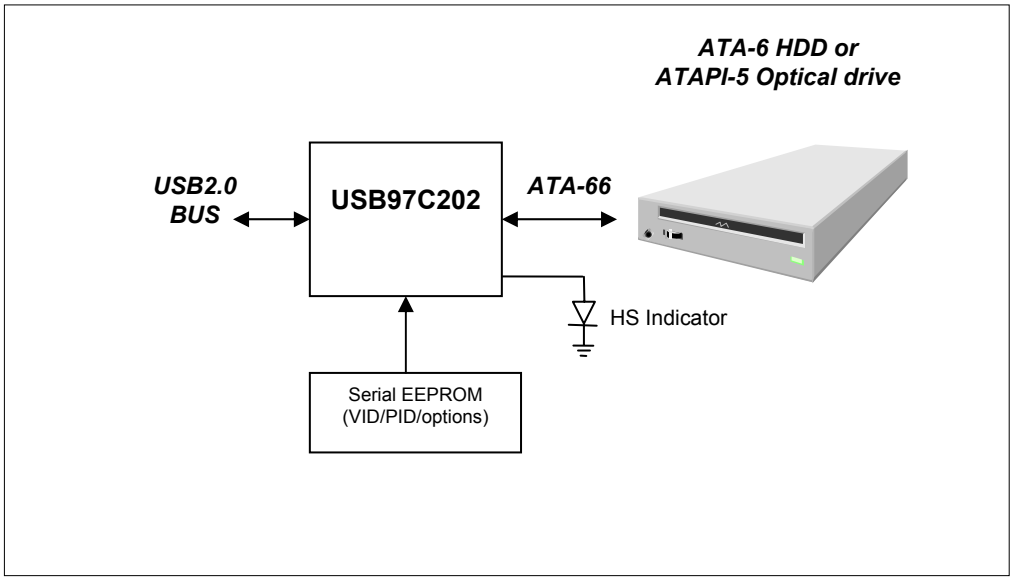
The USB97C202 is a USB2.0 Mass Storage Class Peripheral Controller intended for use with standard ATA-5 and -6 hard drives and standard ATAPI-5 devices.

The device consists of a USB2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad and 768 of program SRAM, internal 48 KB program ROM, and an ATA-66 compatible interface.

Provisions for optional external Flash Memory up to 64K bytes for program storage is provided. A serial EEPROM which can be modified via USB from the host provides unique VID/PID/Serial numbers, as well as optional configuration information.

Internal 768 Bytes of scratchpad SRAM are also provided. This internal SRAM can also be used for program storage to implement program upgrade via USB download to external “boot block” Flash program memory, if desired.

Seven GPIO pins are provided for controlling external power control elements and sensing specialized drive functions. Provisions are made to allow dynamic attach and re-attach to the USB bus to allow hot swap of drives to be implemented.



Chapter 2 Pin Table

DISK DRIVE INTERFACE (27 Pins)			
IDE_D0	IDE_D1	IDE_D2	IDE_D3
IDE_D4	IDE_D5	IDE_D6	IDE_D7
IDE_D8	IDE_D9	IDE_D10	IDE_D11
IDE_D12	IDE_D13	IDE_D14	IDE_D15
IDE_nIOR	IDE_nIOW	IDE_IRQ	IDE_DACK
IDE_DRQ	IDE_nCS0	IDE_nCS1	IDE_SA0
IDE_SA1	IDE_SA2	IORDY	
USB INTERFACE (7 Pins)			
USBD+	USBD-	LOOPFLTR	RBIAS
RTERM	FS+	FS-	
MEMORY/IO INTERFACE (28 Pins)			
MD0	MD1	MD2	MD3
MD4	MD5	MD6	MD7
MA0	MA1	MA2	MA3
MA4	MA5	MA6	MA7
MA8	MA9	MA10	MA11
MA12	MA13	MA14	MA15
nMRD	nIOR	nMWR	nIOW
MISC (15 Pins)			
ROMEN	GPIO1/HS	GPIO2/EE_CS	GPIO3/VBUS
GPIO4/EE_DIO	GPIO5/ATA RESET	GPIO6/A16	GPIO7/EE_CLK
XTAL1/CLKIN	XTAL2	nRESET	nTEST0
nTEST2	nTEST2	CLKOUT	
POWER, GROUNDS, and NO CONNECTS (23 Pins)			

Chapter 3 Pin Configuration

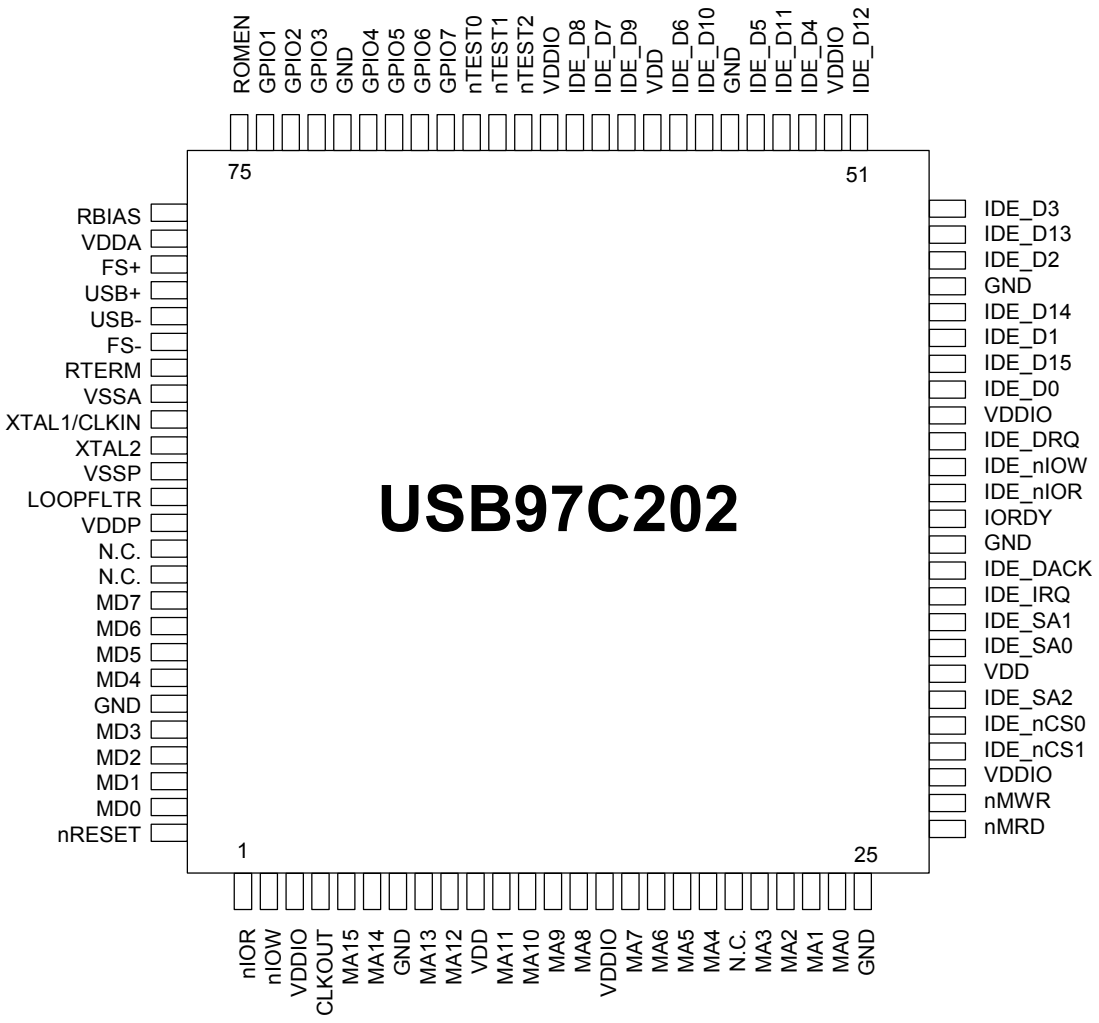
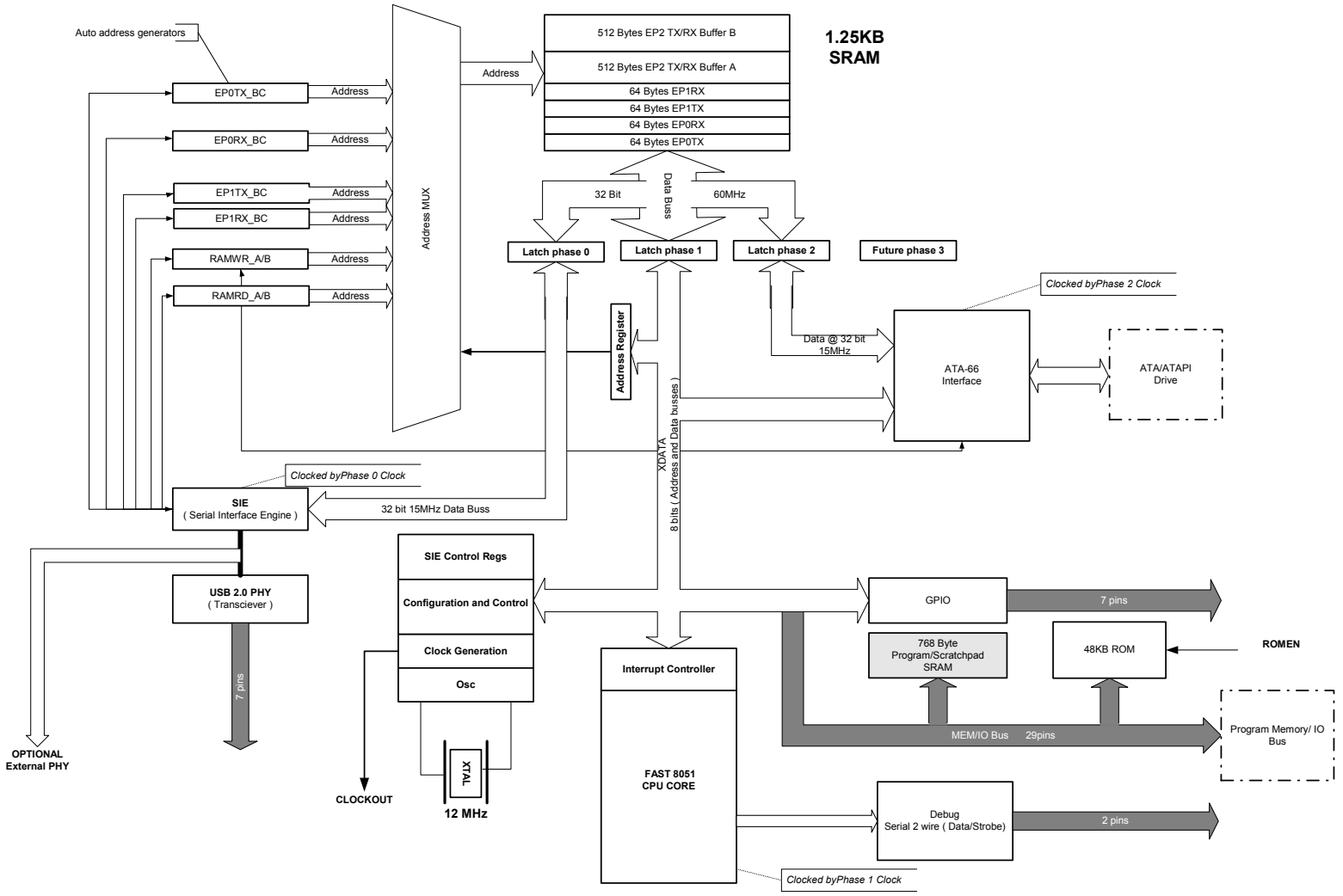


Figure 3.1 - 100 PIN STQFP & TQFP

Chapter 4 Block Diagram



Chapter 5 Pin Descriptions

Table 5.1 - USB97C202 Pin Descriptions

DISK DRIVE INTERFACE			
IDE DMA Request	IDE_DRQ	IS	This pin is the active high DMA request from the ATA/ATAPI interface.
IDE IO Read Strobe	IDE_nIOR	O20	This pin is the active low read signal for the interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Register Address 1	IDE_SA1	O20	This pin is the register select address bit 1 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Register Address 0	IDE_SA0	O20	This pin is the register select address bit 0 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Register Address 2	IDE_SA2	O20	This pin is the register select address bit 2 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Data	IDE_D15	IO20	This pin is the bi-directional data bus bit 15 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE IO Write Strobe	IDE_nIOW	O20	This pin is active low write signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE DMA Acknowledge	IDE_nDACK	O20	This pin is the active low DMA acknowledge signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Interrupt Request	IDE_IRQ	IS	This pin is the active high interrupt request signal for the ATA/ATAPI interface.
IDE Data	IDE_D13	IO20	This pin is the bi-directional data bus bit 13 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Data	IDE_D14	IO20	This pin is the bi-directional data bus bit 14 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*

DISK DRIVE INTERFACE			
IDE Chip Select 0	IDE_nCS0	O20	This pin is the active low chip select 0 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Chip Select 1 0	IDE_nCS1	O20	This pin is the active low select 1 signal for the ATA/ATAPI interface. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IDE Data	IDE_D[0:12]	IO20	These pins are bits 0-12 of the ATA/ATAPI bi-directional data bus. *In part number USB97C202-MN-03 or later ROM codes, this pin is high impedance when VBUS is removed.*
IO Ready	IORDY	I	This pin is the active high IORDY signal from the IDE drive.

USB INTERFACE			
USB Bus Data	USB- USB+	IO-U	These pins connect to the USB bus data signals.
USB Transceiver Filter	LOOPFLTR		This pin provides the ability to supplement the internal filtering of the transceiver with an external network, if required.
USB Transceiver Bias	RBIAS		A *9.09* Kohm precision resistor is attached from ground to this pin to set the transceiver's internal bias currents.
Termination Resistor	RTERM		A precision 1.5Kohm precision resistor is attached to this pin from a 3.3V supply.
Full Speed USB Data	FS- FS+	IO-U	These pins connect to the USB- and USB+ pins through 31.6 ohm series resistors.

MEMORY/IO INTERFACE			
Memory Data Bus	MD[7:0]	IO12PU	When ROMEN=0, these signals are used to transfer data between the internal CPU and the external program memory. When ROMEN=1, a weak internal pull up is activated to prevent these pins from floating.
Memory Address Bus	MA[15:0]	O12	These signals address memory locations within the external memory.
Memory Write Strobe	nMWR	O12	Program Memory Write; active low
Memory Read Strobe	nMRD	O12	Program Memory Read; active low
IO Read Strobe	nIOR	O12	XDATA space Read; active low
IO Write Strobe	nIOW	O12	XDATA space Write; active low

MISC			
Crystal Input/External Clock Input	XTAL1/ CLKIN	ICLKx	12Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 12Mhz clock when a crystal is not used.
Crystal Output	XTAL2	OCLKx	12Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
Clock Output	CLKOUT	O8	This pin produces a 30Mhz clock signal independent of the processor clock divider. It is held inactive and low whenever the internal processor clock is stopped or is being obtained from the ring oscillator.
Internal ROM Enable	ROMEN	IP	When left unconnected or tied high, the USB97C202 uses the internal ROM for program execution. When tied low, an external program memory should be connected to the memory/data bus. The state of this pin latched internally on the rising edge of nRESET.
General Purpose I/O	GPIO[1:7]	IO20	These general purpose pins may be used either as inputs, edge sensitive interrupt inputs, or outputs. When using internal ROM mode, these pins have the following assignments: GPIO1: USB HS Indicator; active high. In part number USB97C202-MN-03 or later ROM codes, this pin also goes high during USB data transfers. GPIO2: Serial EEPROM (93LC66 type) Chip Select GPIO3: USB VBUS Detect Input GPIO4: Serial EEPROM Data In/OutGPIO5: ATA Drive Reset GPIO6: A16 control line for external program Flash memory when using firmware upgrade capability (external ROM operation only) GPIO7: Serial EEPROM Clock output
RESET input	nRESET	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 100ns wide.
Test input	nTEST[0:2]	IP	These signals are used for testing the chip. User should normally leave them unconnected. For board continuity testing, all pads (except RBIAS, FSDP, USBDP, USBDM, FSDM, RTERM, XTAL1, XTAL2, LOOPFLTR and nTEST[0:2]) are included in an XNOR chain which is enabled by pulling nTEST2 low. nIOR is the output of the chain (the chain begins at pin 2) and will reflect the toggling of a signal on each pin. Circuit board continuity of the pin solder connections after assembly can be checked in this manner

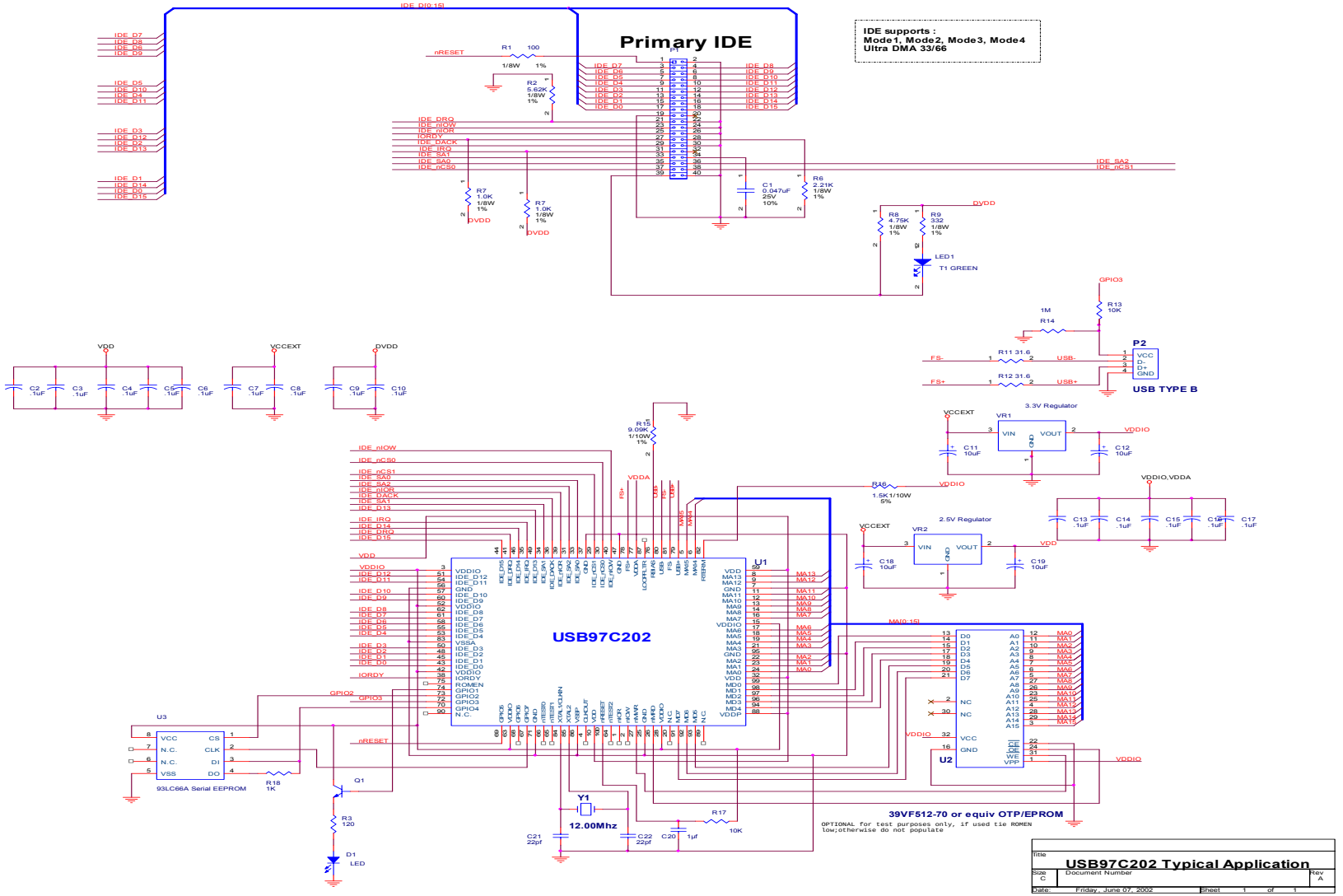
POWER, GROUNDS, and NO CONNECTS			
	VDD		+2.5V Core power
	VDDIO		+3.3V I/O power
	VDDP		+2.5 Analog power
	VSSP		Analog Ground Reference
	VDDA		+3.3V Analog power
	VSSA		Analog Ground Reference
	GND		Ground Reference
	NC		No Connect. These pins should not be connected externally.

5.1 Buffer Type Descriptions

Table 5.2 - USB97C202 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IS	Input with Schmitt trigger
IP	Input with weak pull-up
IO8	Input/Output with 8 mA drive
O8	Output with 8mA drive
O12	Output with 12mA drive
IO12PU	Input/Output with 12 ma drive and controlled weak pull up
IO12	Input/Output with 12 ma drive
IO20	Input/output with 20mA drive
O20	Output with 20mA drive
O20PU	Output with 20mA drive and weak pullup
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Defined in USB specification

Chapter 6 Typical Application



Chapter 7 DC Parameters

7.1 Maximum Guaranteed Ratings

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to Ground 5.5V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum $V_{DDA,}$ V_{DDIO} ..... +4.0V
Maximum $V_{DD,}$ V_{DDP} ..... +3.0V

*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

Table 7.1 - DC Electrical Characteristics
(T_A = 0°C - 70°C, $V_{DDIO,}$ V_{DDA} = +3.3 V ± 10%, $V_{DD,}$ V_{DDP} = +2.5 V ± 10%,)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	uA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	uA	V_{IN} = V_{DDIO}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{DDIO} (Note 7.1)
I/O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (Note 7.1, Note 7.3)
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (Note 7.1, Note 7.3)
I/O20 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 20 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -5 mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (Note 7.1, Note 7.3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO-U **Note 7.2**						
Supply Current Unconfigured	I_{CCINIT}		65 85		mA mA	V_{DDIO}, V_{DDA} V_{DD}, V_{DDP}
Supply Current Active	I_{CC}			85 120	mA mA	V_{DDIO}, V_{DDA} V_{DD}, V_{DDP}

Note 7.1 Output leakage is measured with the current pins in high impedance.

Note 7.2 See appendix A for USB DC electrical characteristics.

Note 7.3 Output leakage is valid only on pins without internal weak pull ups or pull downs.

7.1.1 Capacitance T_A = 25°C; FC = 1MHz; V_{DD} = 2.5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 8 AC Specifications

8.1 ATA/ATAPI

The USB97C202 conforms to all timing diagrams and specifications for ATAPI-5 as set forth in the T13/1321D Revision 3 NCITS specification. Please refer to this specification for more information.

8.2 USB2.0 Timing

The USB97C202 conforms to all timing diagrams and specifications for USB peripheral silicon building blocks as set forth in the USB-IF USB2.0 specification. Please refer to this specification for more information.

Chapter 9 Package Outlines

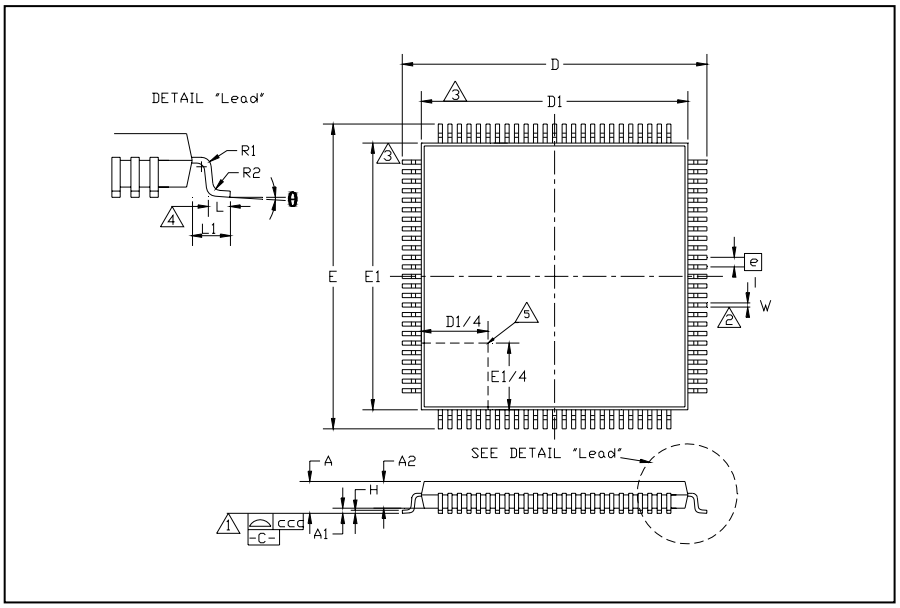


Figure 9.1 - 100 Pin STQFP Package Outline, 12x12x1.4 Body, 2MM Footprint (Rev A)

Table 9.1 - 100 Pin STQFP Package Parameters (Rev A)

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	13.80	~	14.20	X Span
D1	11.80	~	12.20	X body Size
E	13.80	~	14.20	Y Span
E1	11.80	~	12.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.16	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.035 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion.
   Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

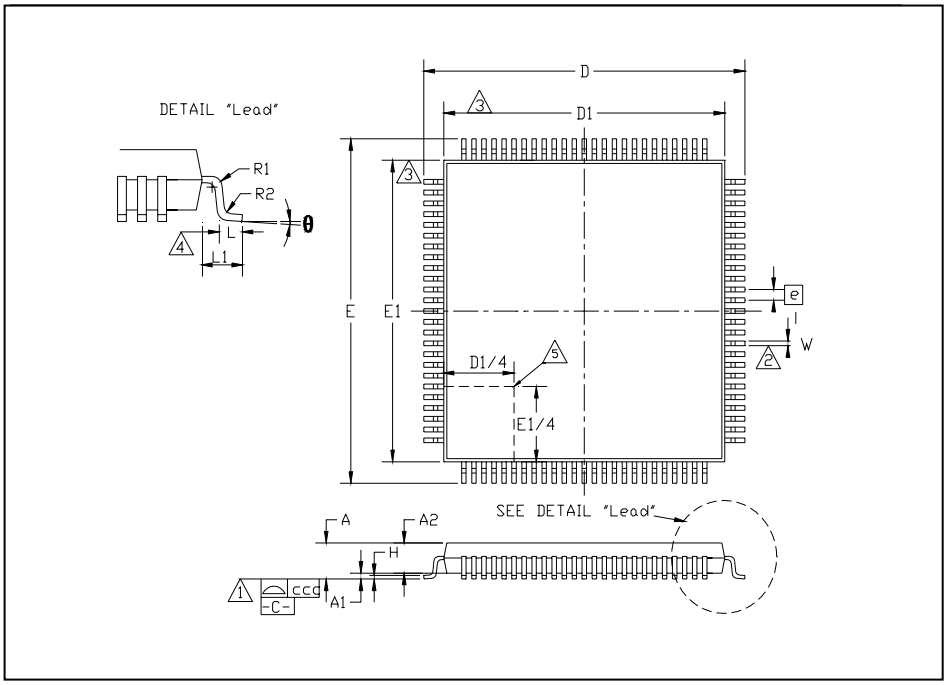


Figure 9.2 - 100 Pin TQFP Package Outline, 14x14x1.4 Body, 2MM Footprint

Table 9.2 - 100 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e		0.50 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:
1. Controlling Unit: millimeter.
2. Tolerance on the position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion.
   Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.