STK6031

8051-based
8-bit microcontroller
with
ISP-programmable
64K flash memory
for application program

V4 2008 Jul 02

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1 FEATURES

- 80C51 Central Processing Unit (CPU).
  - Option for multiple CPU clock (XTAL1, XTAL1 x 2, or XTAL1 / 3).
  - Industrial standard 80C51 instruction set.
  - Normal mode, idle mode, and stop mode.
- Program Memory : 64 kbytes on-chip flash memory.
  - with hardware ISP (In-System Programming).
  - Program code protection.
- Main Data RAM: 256 bytes (upper 128 + lower 128 bytes) of on-chip SRAM.
- Aux Memory (AUX RAM): 768 bytes of SRAM.
- Stretch memory cycle for the MOVX instruction.
- SFRs (Special Function Register): 47 SFRs.
- Timers: Timer 0, Timer 1, and Timer 2.
- On-chip Watchdog Timer.
- Full-duplex UART
- Five I/O ports: Port 0, Port 1, Port 2, Port 3, and Port 4 (P4.0 ~ P4.3).
- On-chip power-on-reset with low-voltage detection and reset.
- Interrupts: 6 sources, 2 priority level, 6 vectored addresses.
- Software enable/disable of ALE output pulse to reduce EMI.
- 4-channel, 6-bit ADC.
- 5-channel, 8-bit PWM.
- CPU operating frequency range: 2 to 30 MHz
- Operating temperature range: -20 to +85°C
- Operating voltage range: 2.7 to 3.6 V.
- ESD: ≥3 KV (HBM).
- Latch-up: 150 mA.
- Reliability of 64K flash memory:
  - Data retention: 10 years at room temperature.
  - Number of read/write cycle: > 20K.
- Available in 3 types of Pb-free package: PLCC44, QFP44, LQFP48.

2 ORDERING INFORMATION

Table 1 Ordering information

TYPE NUMBER	PACKAGE	OUTLINE DRAWING
STK6031APLP	PLCC44 (Pb-free)	please refer to Figure 43 on page 100.
STK6031AQPP	QFP44 (Pb-free)	please refer to Figure 44 on page 101.
STK6031ALQP	LQFP48 (Pb-free)	please refer to Figure 45 on page 102.

3 FUNCTIONAL BLOCK DIAGRAM

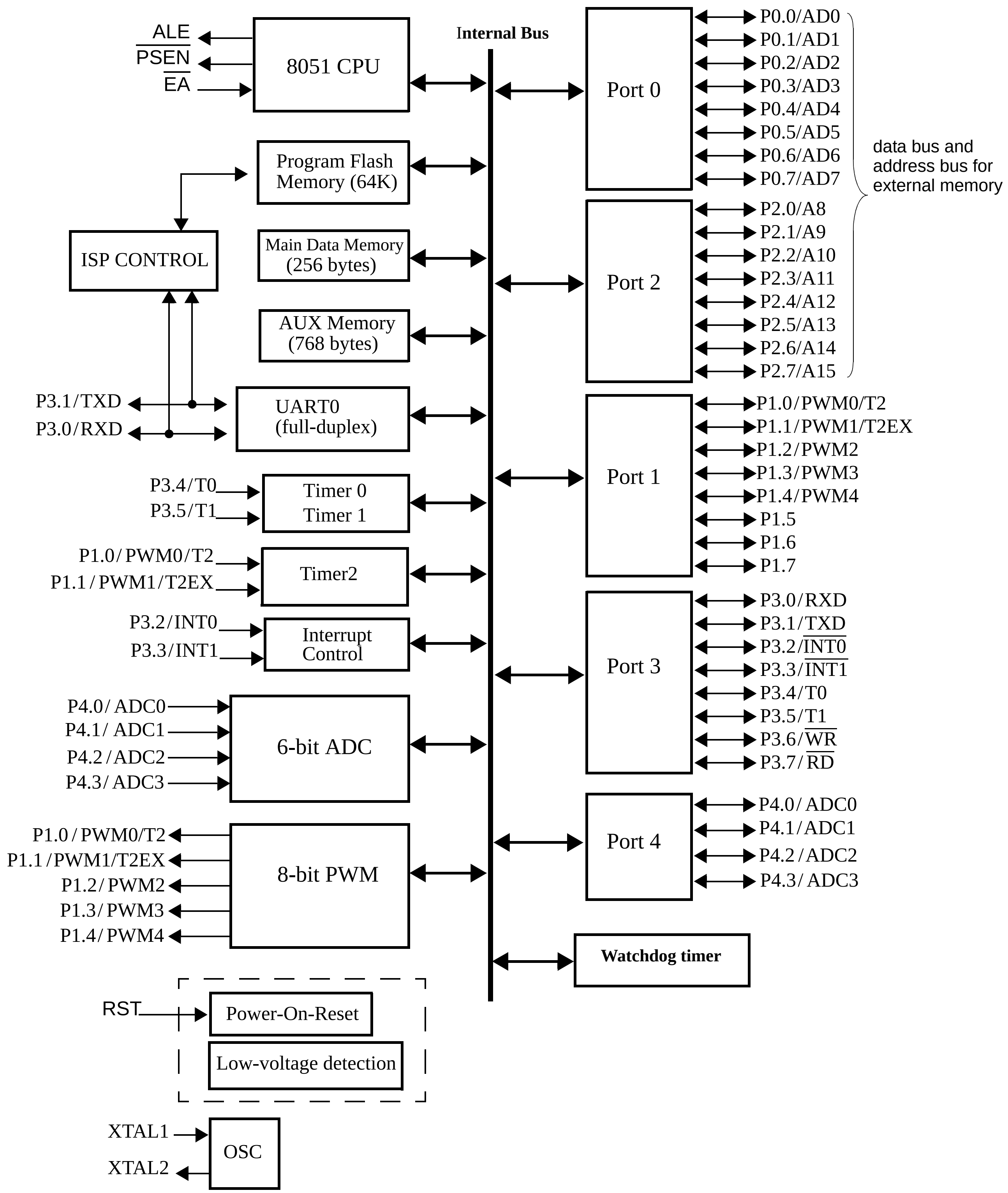


Fig.1 Functional block diagram

4 PINNING INFORMATION

4.1 Pinning diagram(QFP44 package)

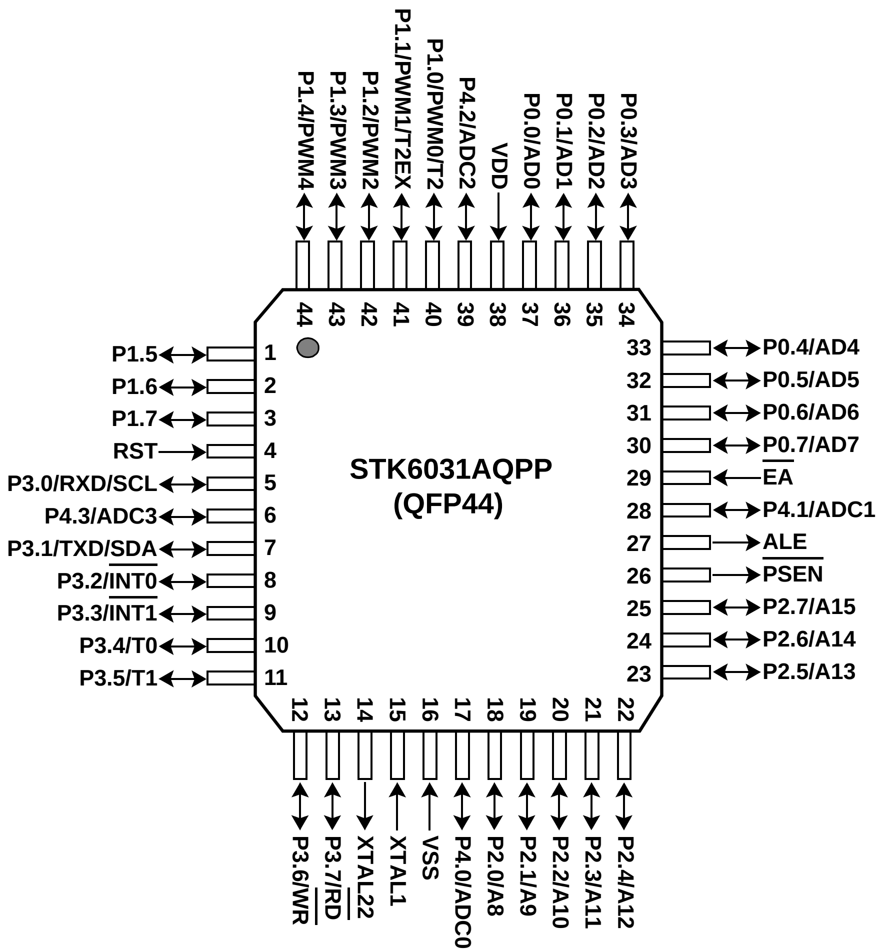


Fig.2 Pin configuration of QFP44 package.

4.2 Pinning diagram(LQFP48 package)

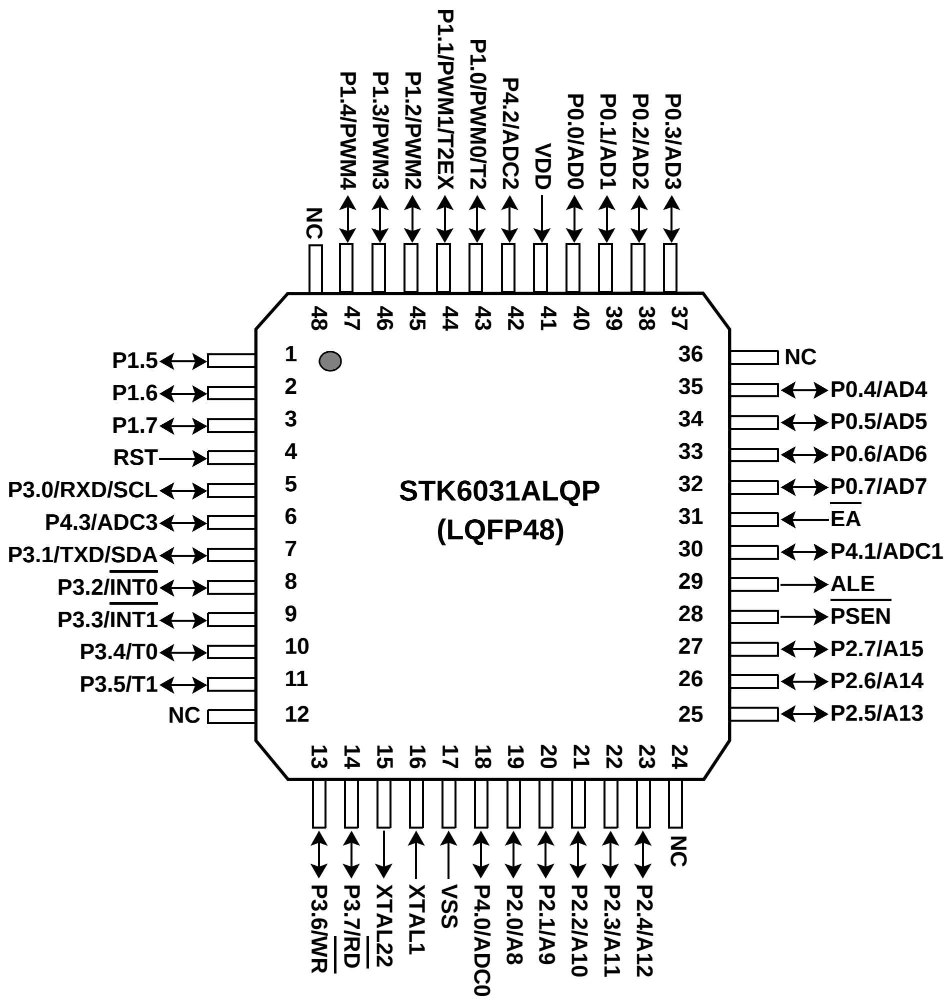


Fig.3 Pin configuration of LQFP48 package.

4.3 Pinning diagram(PLCC44)

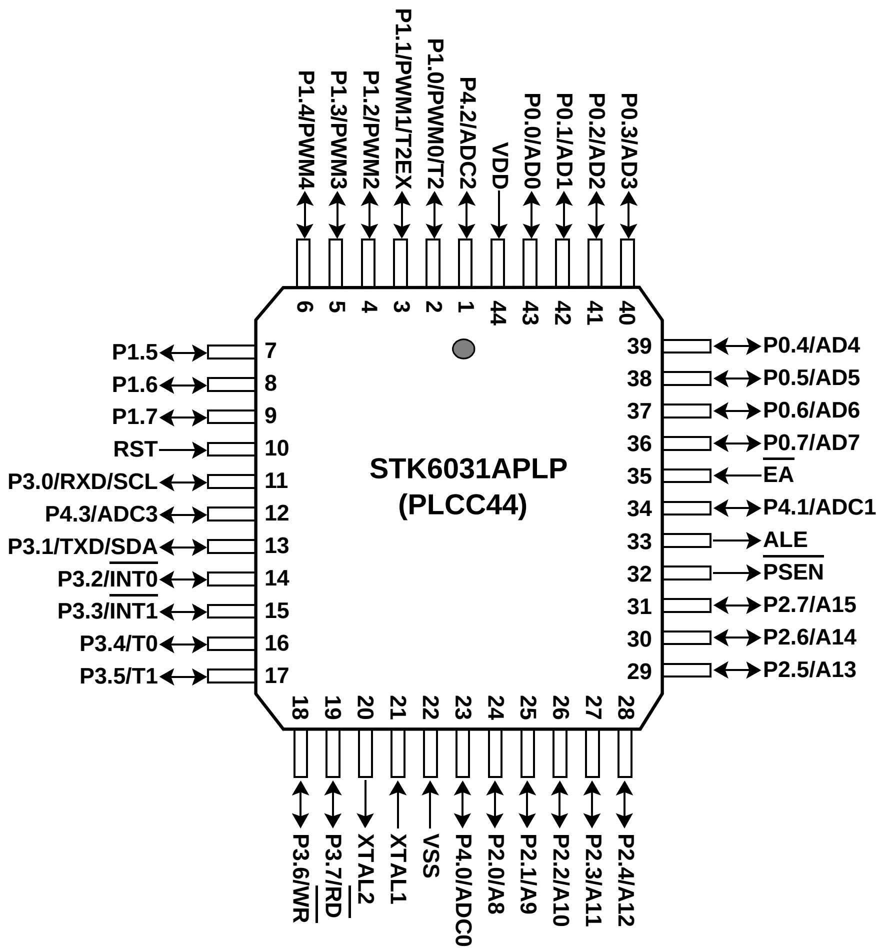


Fig.4 Pin configuration of PLCC44 package.

4.4 Pin description

Table 2 Pin description for QFP44 package

To avoid a latch-up effect at power-on: V_{SS} – 0.5 V < voltage at any pin at any time < V_{DD} + 0.5 V .

SYMBOL	PIN	TYPE	DESCRIPTION
P1.5, P1.6, P1.7	1~3	I/O	Bits 5, 6, 7 of Port 1. These pins are pure I/O pins.
RST	4	I	External reset input pin, active HIGH. A HIGH level on this pin for at least 8 XTAL1 clocks, while the oscillator is running, resets the STK6031.
P3.0/RXD/SCL	5	I/O	Bit 0 of Port 3, or data receiver pin of the UART, or clock pin for ISP programming.
P4.3/ADC3	6	I/O	Bit 3 of Port 4 or the third channel input of the 6-bit ADC.
P3.1/TXD/SDA	7	I/O	Bit 1 of Port 3, data transmitter pin of the UART, or data pin for ISP programming.
P3.2/$\overline{INT0}$	8	I/O	Bit 2 of Port 3 or input of External Interrupt 0.
P3.3/$\overline{INT1}$	9	I/O	Bit 3 of Port 3 or input of External interrupt 1.
P3.4/T0	10	I/O	Bit 4 of Port 3 or Timer 0 input.
P3.5/T1	11	I/O	Bit 5 of Port 3 or Timer 1 input.
P3.6/$\overline{WR}$	12	I/O	Bit 6 of Port 3 or external AUX data memory write strobe. When selected as write strobe to external AUX RAM, the function of P3.6 is disabled.
P3.7/$\overline{RD}$	13	I/O	Bit 7 of Port 3, or external AUX data memory read strobe. When selected as read strobe to external AUX RAM, the function of P3.7 is disabled.
XTAL2	14	O	**Crystal pin 2:** output of the inverting amplifier that forms the oscillator. This pin should be left open-circuit when an external oscillator clock is used.
XTAL1	15	I	**Crystal pin 1:** input to the inverting amplifier that forms the oscillator. Receives the external oscillator clock signal when an external oscillator is used.
VSS	16	I	Ground pin.
P4.0/ADC0	17	I/O	Bit 0 of Port 4 or channel 0 input of the 6-bit ADC.
P2.0/A8~ P2.7/A15	18~25	I/O	Port 2, or Address 8~15 when fetching external program ROM or read/write external AUX data memory. Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-up PMOS and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the internal pull-up PMOS. Port 2 sends out the high-order address (A8 ~ A15) during read from external program memory and during read/write access to external AUX data memory, using 16-bit address lines (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s.
$\overline{PSEN}$	26	O	Program Strobe Enable This is read strobe to external program memory. When the CPU is executing code coming from external program memory, $\overline{PSEN}$ is activated once each instruction cycle. Please refer to Fig.42 for external program memory read timing.

SYMBOL	**PIN**	**TYPE**	**DESCRIPTION**
ALE	27	O	Address Latch Enable Output pulse for latching the low byte of the address during an access to external program memory or AUX data memory. In normal operation, ALE is sent out at a constant rate of 1/4 oscillator frequency, and can be used for external clocking or timing. Note that, when executing a stretched MOVX instruction, CPU will send out two ALE pulses. The ALE output can be disabled by setting bit 3 (ALEDIS) of SFR CHIPCON at location BF(hex) to HIGH. With this bit set to HIGH, the pin is weakly pulled high. The ALE disable feature is terminated by reset. Setting the ALEDIS bit has no effect, if the CPU is in external memory access mode.
P4.1/ADC1	28	I/O	Bit 1 of Port 4 or channel 1 input of the on-chip ADC.
$\overline{EA}$	29	I	External Access Enable. The CPU checks this input **during power-on reset**. If $\overline{EA}$=0, the CPU fetches instruction from external (off-chip) program memory. If $\overline{EA}$=1, the CPU fetches instructions from internal (on-chip) program memory.
P0.0/AD0~ P0.7/AD7	30~3 7	I/O	Port 0, Address 0~7 or Data 0~7 when CPU performs a read from external program memory, or a read/write operation to external AUX data memory. Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program memory or AUX memory. In this application, it uses strong internal pull-ups when emitting 1s.
VDD	38		Power supply.
P4.2/ADC2	39	I/O	Bit 2 of Port 4 or channel 2 input of the 6-bit ADC.
P1.0/PWM0/T2	40	I/O	This pin has four functions: • Bit 0 of Port 1, • PWM0 output, • clock input for Timer 2,or • pulse output of Timer 2, when it is in Programmable Clock Output mode.
P1.1/PWM1/T2EX	41	I/O	Bit 1 of Port 1, PWM1 output, or T2EX input of Timer 2.
P1.2/PWM2, P1.3/PWM3, P1.4/PWM4	42, 43, 44	I/O	Bit 2, 3, 4 of Port 1 or outputs PWM 2, 3,4 of the Pulse Width Modulator.

5 CENTRAL PROCESSING UNIT (CPU)

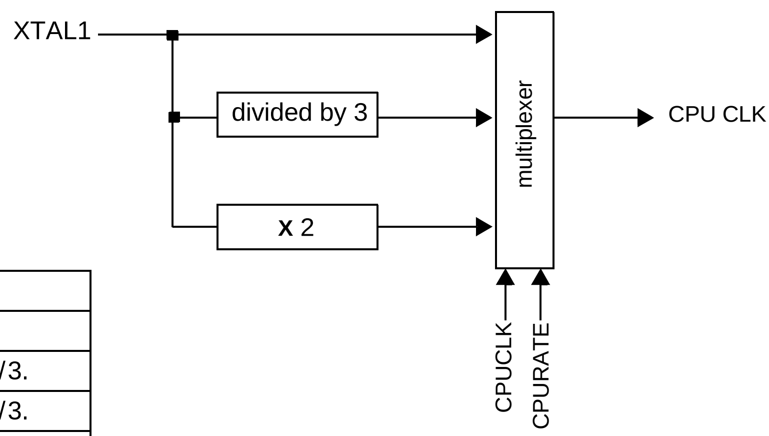
5.1 Instruction Set and addressing modes

The STK6031's instruction set and addressing modes are completely compatible with that of industrial standard 80C51. User codes written in traditional 80C51 instruction set can be ported directly to the STK6031. However, due to difference in CPU instruction clocks and timing, applications in which timer loops are used may need modification in the number of loops.

For a description of instruction set, please refer to Chapter 28, *Instruction set*.

5.2 CPU clock and Chip Configuration Register (SFR CHIPCON)

The STK6031 can be configured to run at different clock frequencies by use of bit 2 and bit 1 of the Chip Configuration Register (SFR CHIPCON), as illustrated in Fig.5.



CPU clock control

CPUCLK	CLKRATE	CPU CLK
0	0	CPU CLK=XTAL1
0	1	CPU CLK=XTAL1/3.
1	1	CPU CLK=XTAL1/3.
1	0	CPU CLK=XTAL1X2.

Note: The default after power-on-reset is: CPU CLK = XTAL1.

Fig.5 CPU clock

The Chip Configuration Register (SFR CHIPCON, at SFR map address BF hex) controls the following:

- Enable or disable the on-chip AUX memory access,
- Enable or disable of the ALE output,
- Selection of CPU clock, and
- Enable or disable of low-power reset.

Table 3 Chip Configuration Register

Chip Configuration Register (SFR CHIPCON), located at BF hex of the SFR map, Read/Write								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	x	x	x	XRAMEN	ALEDIS	CPUCLK	CLKRATE	LVR
Reset value	x	x	x	1	0	0	0	0

Table 4 Description of Chip Configuration Register (CHIPCON)

MNEMONIC	BIT POSITION	FUNCTION
	Bits 5, 6, 7	Not implemented.
XRAMEN	CHIPCON.4	Enable or disable of the on-chip AUX memory access. • XRAMEN= 1 enables the read/write access to the on-chip AUX memory. • XRAMEN= 0 disable the read/write access to the address AUX memory.
ALEDIS	CHIPCON.3	Disable of the ALE output. • When ALEDIS=1, the ALE Disable is turned on, that is, the ALE output will not toggle and EMI can be lowered. • When ALEDIS=0, the ALE output toggles.
CPUCLK	CHIPCON.2	These two bits are used to select the CPU clock frequency. The CPU clock can be selected to be XTAL1, XTAL1÷3, or XTAL1**x**2. The default after power-on-reset is: CPU CLK = XTAL1. Please refer to Fig.5. for detail.
CLKRATE	CHIPCON.1	
LVR	CHIPCON.0	Enable the low-voltage reset function. • LVR=0 enables the low-voltage reset function. • LVR=1 disables the low-voltage reset function.

5.3 Instruction Cycle

The following diagram illustrates the relation among system clock (CPU CLK), instruction cycle, CPU cycle, and ALE. Simple instructions can be executed in just one instruction cycle, which consists of 4 CPU clocks.

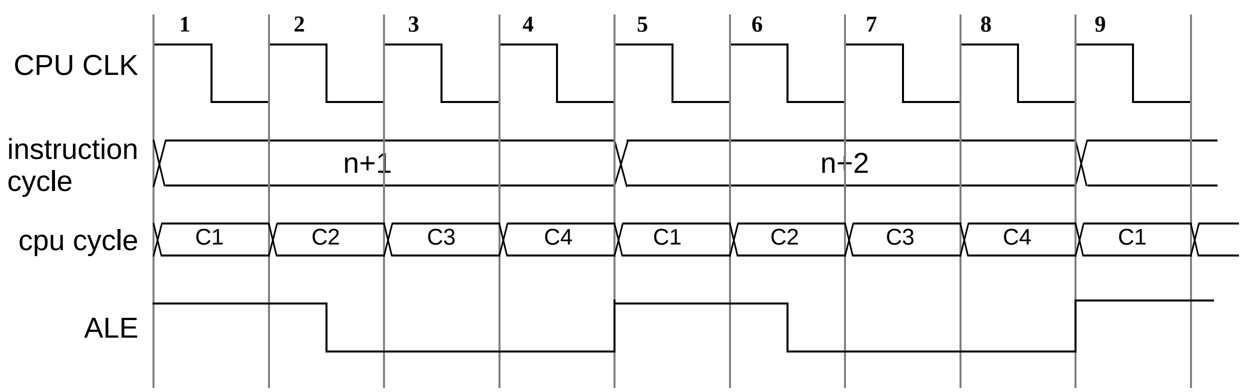


Fig.6 CPU timing for single-cycle instruction.

5.4 Program Status Word

The current state of the CPU is reflected in the Program Status Word (PSW) register, which is located at SFR address D0(hex).

Table 5 Program Status Word

PROGRAM STATUS WORD (SFR PSW), LOCATED AT D0H OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	CY	AC	F0	RS1	RS0	OV	F1	P

Table 6 Description of Program Status Word (PSW)

MNEMONIC	BIT POSITION	FUNCTION
CY	PSW.7	Carry flag. The Carry flag receives Carry-out from bit 7 of ALU. It is set to HIGH, when last arithmetic operation resulted in a carry (during addition) or borrow (during subtraction); otherwise, it is cleared to LOW by all arithmetic operations.
AC	PSW.6	Auxiliary Carry Flag. Auxiliary Carry Flag receives Carry-out from bit 3 of addition operands. It is set to HIGH, when last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high-order nibble; otherwise, it is cleared to LOW by all arithmetic operations
F0	PSW.5	General purpose flag. This bit is uncommitted and may be used as general purpose status flag.
RS1, RS0	PSW.4, PSW.3	Register Bank select control bits. • RS1, RS0 = 00 selects register bank 0, address 00h ~ 07h. • RS1, RS0 = 01 selects register bank 1, address 08h ~ 0Fh. • RS1, RS0 = 10 selects register bank 2, address 10h ~ 17h. • RS1, RS0 = 11 selects register bank 3, address 18h ~ 1Fh.
OV	PSW.2	Overflow flag. This bit is set to HIGH, when last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide); otherwise, it is cleared to LOW by all arithmetic operation.
F1	PSW.1	General purpose flag. This bit is uncommitted and may be used as general purpose status flag.
P	PSW.0	Parity flag. Set/Clear by hardware each instruction cycle to indicate an odd/even number of 1s in the accumulator, i.e., even parity.

6 MEMORY ORGANIZATION

The STK6031 has 4 blocks of on-chip memories. These are:

- 65536 bytes of flash program memory,
- 256 bytes of Main Data Memory,
- 768 bytes of AUX memory, and
- 46 bytes of Special Function Register.

The following diagram shows the overall memory spaces available in the microcontroller.

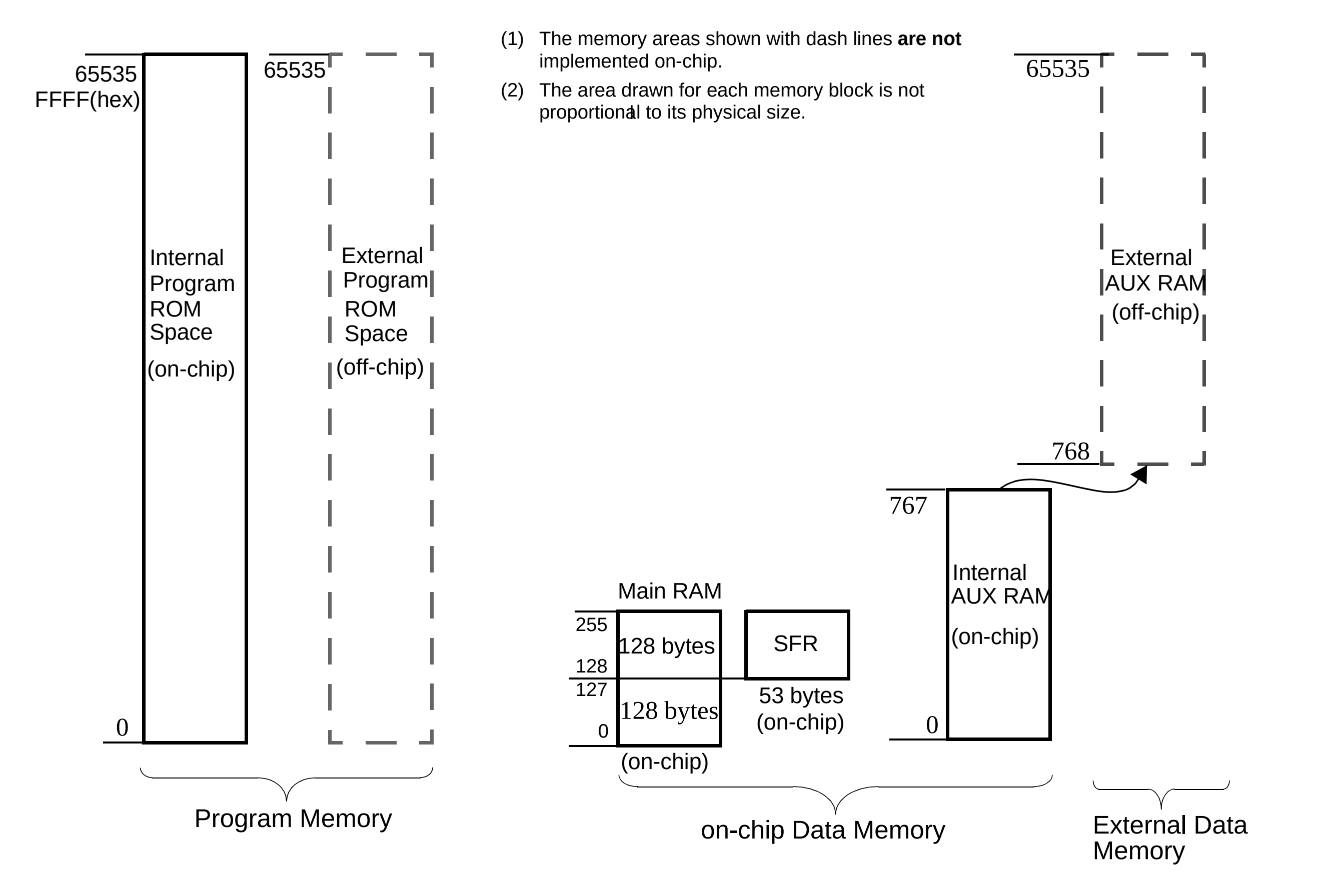


Fig.7 The overall memory space

6.1 Program Memory

6.1.1 PROGRAM ROM SPACE

The STK6031 CPU fetches instructions either from the on-chip program memory or the off-chip program memory. For both memories, the address range is from 0000(hex) to FFFF(hex).

6.1.2 ON-CHIP PROGRAM MEMORY VERSUS EXTERNAL PROGRAM MEMORY

If, during reset, the $\overline{EA}$ (External Access) pin, is held HIGH, the STK6031 always executes out of the on-chip Program Memory. If the $\overline{EA}$ pin is held LOW during reset, the STK6031 fetches instructions from off-chip Program Memory. The $\overline{EA}$ input is latched during reset and is ignored after reset. After reset, the CPU starts fetching program ROM code at location 0000H.

The off-chip memory is accessed via Port 0 and Port 2.

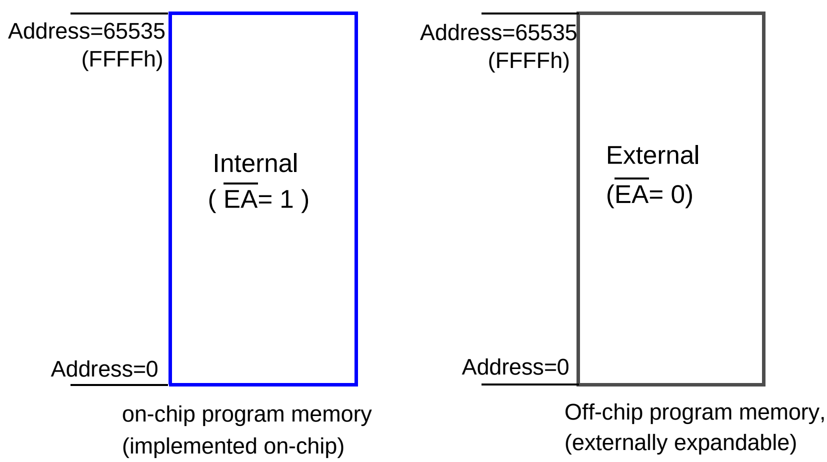


Fig.8 Program Memory.

6.1.3 ISP PROGRAMMING FOR THE 64K FLASH MEMORY

The on-chip program memory is implemented using flash memory, with ISP (In-System Programming) capability. Detailed description of ISP programming is given in another document.

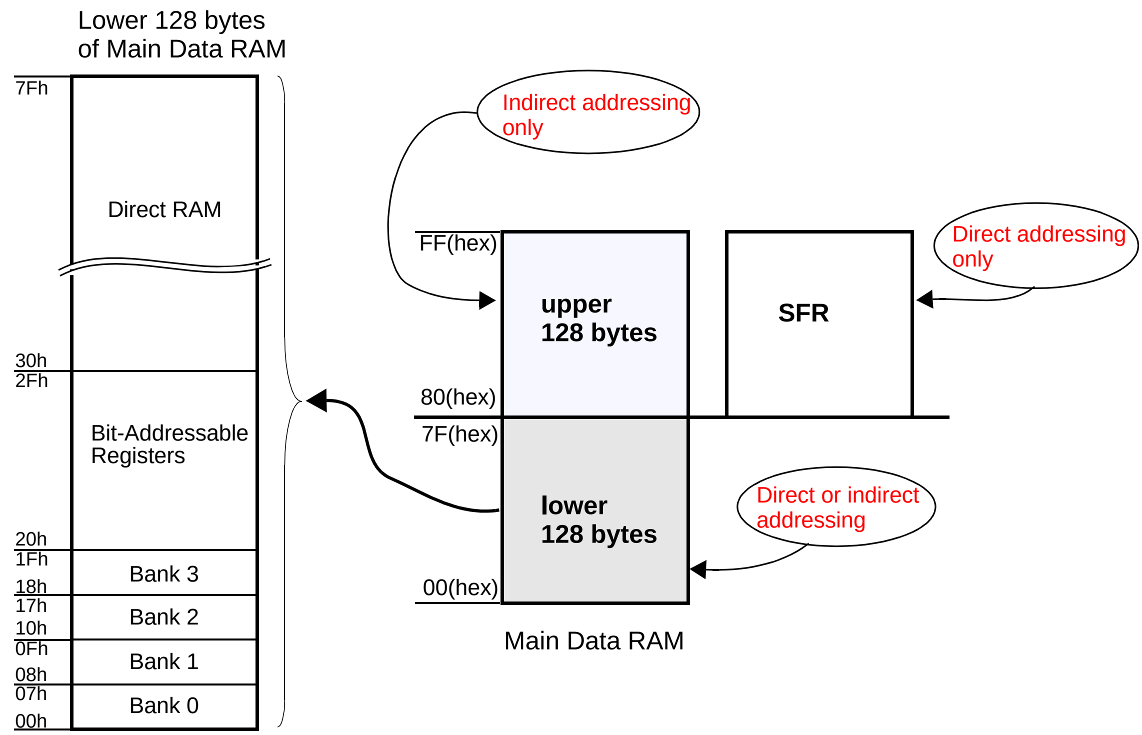
6.1.4 ROM CODE PROTECTION

ROM code protection is implemented in the 64K flash memory.

6.2 Main Data RAM and Special Function Register (SFR)

The STK6031 has 256 bytes of on-chip Main Data RAM and 53 bytes of SFR. Although the Main Data RAM and the SFRs shares overlapped memory space, they are two physically separate blocks. The upper 128 bytes of the Main Data RAM, from address 80H to FFH can be accessed only by **Indirect Addressing**. The lower 128 bytes of the Main RAM, from address 00H to 7FH, can be accessed by **Direct Addressing** or **Indirect Addressing**.

The SFRs occupy the address range from 80H to FFH and are only accessible using **Direct Addressing**.



PSW SFR		
Bit 4	Bit 3	selected bank
1	1	3
1	0	2
0	1	1
0	0	0

Fig.9 Main Data Memory and SFRs

6.2.1 THE LOWER 128 BYTES OF THE MAIN DATA RAM

The lower 128 bytes are organized as shown in Fig.9. The lower 32 bytes form 4 banks of eight registers (R0 - R7). Two bits on the Program Status Word (PSW) select which bank is active (in use). The next 16 bytes, from 20 (hex) to 2F (hex) , form a block of bit-addressable memory space, at bit address 00(hex) ~ 07(hex).

6.3 AUX Memory

6.3.1 AUX MEMORY SPACE

The STK6031 has 64K bytes of auxiliary memory (AUX RAM) space, which can be accessed by executing MOVX instruction. The AUX RAM space is physically divided into two blocks: the on-chip block and the off-chip block. The on-chip block has a capacity of 768 bytes and starts from address 0 to address 767(decimal). The off-chip block starts from address 768(decimal) to address 65535.

The MOVX @Ri instruction, where i=0 or 1, can access only the lowest 256-bytes of the on-chip AUX RAM. The MOVX @DTPR instruction can access the whole range of the AUX RAM space.

AUX RAM space from address 768 to address 65535 is allocated as external AUX RAM and can only be accessed by the MOVX @DPTR instruction. The external AUX RAM is externally expandable, with Port 0 used as low-byte address/data, Port 2 used as high-byte address, P3.6 used as Write strobe, and P3.7 used as Read strobe.

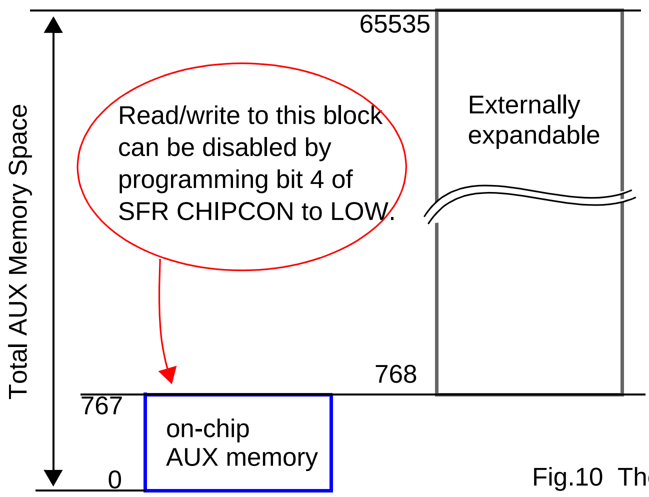


Fig.10 The AUX Memory Space

6.3.2 ON-CHIP AUX MEMORY

The on-chip AUX RAM from address 0 to address 767 can be accessed by the CPU as normal data memory, by performing a MOVX instruction. Read/Write access to this memory can be disabled by setting bit 4 of the SFR CHIPCON to LOW. Please refer to Table 3 and Table 4 for detailed description of the SFR CHIPCON.

When executing MOVX instruction from internal program memory, an access (read or write) to the internal AUX RAM will not affect the status of Port 0, Port 2, P3.6(write) and P3.7.(read).

6.3.3 DUAL DATA POINTER (DATA POINTER 0 AND DATA POINTER 1) AND DPTR SELECT REGISTER (SFR DPS)

The STK6031 has two data pointers, Data Pointer 0 and Data Pointer 1. Data Pointer 0 is the traditional 8051 data pointer for MOVX instrucitons. Data Pointer 1 is an extra data pointer for fast moving a block of data. Before executing a MOVX instruction, an active data pointer must be selected by programming the Data Pointer Select Register (SFR DPS). Please refer to Table 7 for detailed description of SFR DPS.

Table 7 Data Pointer 0, Data Pointer 1, and DPTR Select Register

Address (Hex)	R/W	SYMBOLS	DESCRIPTION	Reset Value
82	R/W	DPL0	Data Pointer 0 Low (traditional 80C51 data pointer)	0000 0000
83	R/W	DPH0	Data Pointer 0 High (traditional 80C51 data pointer)	0000 0000
84	R/W	DPL1	Data Pointer 1 Low (extra data pointer), specific to the STK6031.	0000 0000
85	R/W	DPH1	Data Pointer 1 High (extra data pointer), specific to the STK6031.	0000 0000
86	R/W	DPS	DPTR Select Register (DPS), specific to the STK6031. The DPS register has only one bit. Only its bit 0, called SEL bit, is implemented on-chip. When SEL=0, instructions that use the DPTR will use SFR DPL0 and SFR DPH0. When SEL=1, instructions that use the DPTR will use SFR DPL1 and SFR DPH1. Bits 7~1 of SFR DPS can not be written to, and, when read, always return a 0 for any of these 7 bits.	0000 0000

All DPTR-related instrucitons use the currently selected data pointer. To switch the active pointer, toggle the SEL bit, by use of the instruction INC DPS. The 6 instructions that use the DPTR are given in the following table. An active DPTR must be selected before executing these instructions.

Table 8 Instructions that use the DPTR

INSTRUCTION	DESCRIPTION
INC DPTR	Increment the data pointer by1.
MOV DPTR, #data16	Load the DPTR with a 16-bit constant.
MOV A, @ A+DPTR	Move code byte relative to DPTR to Accumulator (ACC).
MOVX A, @DPTR	Move AUX Memory byte (16-bit address) to Accumulator (ACC)
MOVX @DPTR, A	Move ACC to AUX memory byte.
JMP @ A+DPTR	Jump indirect relative to DPTR.

6.3.4 Stretch Memory Cycles for accessing external AUX memory and Clock Control Register

By default (after a reset), the MOVX instruction is executed in 3 instruction cycles. However, it is possible to shorten or lengthen, dynamically by user program, the instruction cycles needed to execute a MOVX instruction, by use of the M2, M1, and M0 bits of the Clock Control Register (SFR CKCON).

The added extra cycles affects the width of the read/write strobe and all related timing. Using a higher stretch value results in a wider read/write strobe, which then allows the memory more time to respond.

Table 9 and Table 10 give description of the Clock Control Register and Table 11 gives description about the stretched cycles for various values of M2, M1, and M0.

Table 9 Clock Control Register, SFR CKCON

Clock Control Register (SFR CKCON), located at 8E(hex) of the SFR map								
Bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonics	Reserved		T2M	T1M	T0M	MD2	MD1	MD0
Reset value	0	0	0	0	0	0	0	1

Table 10 Description of the CKCON Register

MNEMONIC	BIT POSITION	FUNCTION
T2M	CKCON.5	Select Timer 2 clock frequency. When T2M=0, Timer 2 uses (CPU CLK / 12) as clock frequency. When T2M=1, Timer 2 uses (CPU CLK / 4) as clock frequency.
T1M	CKCON.4	Select Timer 1 clock frequency. When T1M=0, Timer 1 uses (CPU CLK / 12) as clock frequency. When T1M=1, Timer 1 uses (CPU CLK / 4) as clock frequency.
T0M	CKCON.3	Select Timer 0 clock frequency. When T0M=0, Timer 0 uses (CPU CLK / 12) as clock frequency. When T0M=1, Timer 0 uses (CPU CLK / 4) as clock frequency.
MD2	CKCON.2	Control the number of cycles to be used for accessing external AUX memory, using the MOVX instruction.
MD1	CKCON.1	
MD0	CKCON.0	

Table 11 Data Memory Stretch Values for the MOVX instruction

MD2	MD1	MD0	Instruction cycles for executing MOVX	Read/Write Strobe Width (CPU CLK)	Strobe Width Time @25 MHz
0	0	0	2	2	80 ns
0	0	1	3 (default)	4	160 ns
0	1	0	4	8	320 ns
0	1	1	5	12	480 ns
1	0	0	6	16	640 ns
1	0	1	7	20	800 ns
1	1	0	8	24	960 ns
1	1	1	9	28	1120 ns
Assume that XTAL1=CPU CLK. Please refer to Fig.5.					

7 INTERRUPTS

7.1 General Description

The STK6031 support s 6-source, 2-level, 6 vectored-address interrupt system. Interrupts come from the sources listed below:

- External interrupt 0
- External interrupt 1
- Timer 0 overflow
- Timer 1 overflow
- Timer 2 overflow or External event
- Transmission or reception of the UART

Each interrupt can be individually enabled or disabled and can be assigned a low-level or high-level priority. All interrupts can be globally disabled. When an interrupt event occurs, its corresponding interrupt flag is raised to HIGH. This flag should be cleared by the user interrupt service routine.

In addition to being assigned a low level or a high-level, interrupts within a level have a natural priority level, as shown in Table 12.

Table 12 gives an overview of the interrupt system.

Table 12 Overview of the interrupt system

Source number	**Interrupt sources**	**Flags generated by the interrupt**	**Interrupt enable bit**	**Interrupt priority bit**	**Priority within level**	**Vector Address**
1	External Interrupt 0	IE0 (TCON.1)	EX0 (IE.0)	PX0 (IP.0)	1 (the highest)	0003H
2	Timer 0 Overflow	TF0 (TCON.5)	ET0 (IE.1)	PT0 (IP.1)	2	000BH
3	External Interrupt 1	IE1 (TCON.3)	EX1 (IE.2)	PX1 (IP.2)	3	0013H
4	Timer 1 Overflow	TF1 (TCON.7)	ET1 (IE.3)	PT1 (IP.3)	4	001BH
5	UART Interrupt (UART receive or transmit)	TI (SCON0.1)	ES (IE.4)	PS (IP.4)	5	0023H
		RI (SCON0.0)				
6	Timer 2 overflow	TF2 (T2CON.7)	EX2 (IE.5)	PT2 (IP.5)	6	002BH
	T2EX pin	EXF2 (T2CON.6)				

Note:

1. Because Timer2 overflow and T2EX share the same interrupt vector address 002BH, it is the responsibility of software programmer to check individual interrupt flag to see which one caused the interrupt.

7.2 Interrupt Enable Registers

Each of the interrupt sources can be individually enabled or disabled by setting its enable/disable bit in the Interrupt Enable Registers (SFR IE), located at A8 (hex) of the SFR map. All interrupts can be globally disabled by clearing the EA bit of SFR IE.

The Interrupt Enable Register is described in Table 13 and Table 14.

Table 13 Interrupt Enable Register SFR IE

INTERRUPT ENABLE REGISTER (SFR IE), LOCATED AT A8H OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	EA		ET2	ES0	ET1	EX1	ET0	EX0
Reset value	0	0	0	0	0	0	0	0

Table 14 Description of Interrupt Enable Register SFR IE

MNEMONIC	BIT POSITION	FUNCTION
EA	IE.7	Global enable or disable of all interrupts. When IE.7 = 0, all interrupts are globally disabled. When IE.7 = 1, all interrupt sources are ***globally*** enabled. Please refer to Fig.11 for an overview of the interrupt system.
	IE.6	Not implemented.
EX2	IE.5	Enable or disable interrupt due to Timer 2 overflow, or T2EX pin (shared with P1.1) interrupt. When IE.5 = 1, external interrupt 2 is enabled. When IE.5 = 0, external interrupt 2 is disabled.
ES0	IE.4	Enable or disable UART interrupt. When IE.4 = 1, UART interrupt is enabled. When IE.4 = 0, UART interrupt is disabled.
ET1	IE.3	Enable Timer 1 overflow interrupt. When IE.3 = 1, Timer 1 overflow interrupt is enabled. When IE.3 = 0, Timer 1 overflow interrupt is disabled.
EX1	IE.2	Enable External Interrupt 1. When IE.2 = 1, External Interrupt 1 is enabled. When IE.2 = 0, External Interrupt 1 is disabled.
ET0	IE.1	Enable Timer 0 overflow interrupt. When IE.1 = 1, Timer 0 overflow interrupt is enabled. When IE.1 = 0, Timer 0 overflow interrupt is disabled.
EX0	IE.0	Enable External Interrupt 0. When IE.0 = 1, External Interrupt 0 is enabled. When IE.0 = 0, External Interrupt 0 is disabled.

7.3 Interrupt Priority Register SFR IP

Each interrupt source can be assigned one of two priority levels: high and low. Interrupt priority is defined by the Interrupt Priority Register (SFR IP, at B8 hex of the SFR map), which is described in Table 15 and Table 16.

Interrupt priority levels are as follows:

- logic 0 = low priority
- logic 1 = high priority.

A low priority interrupt may be interrupted by a high priority interrupt. A high priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority occur simultaneously, the high priority level request is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level, there is a second priority structure determined by the polling sequence. This second priority structure is shown in Table 12.

Table 15 Interrupt Priority Register SFR IP

SFR Interrupt Priority Register (SFR IP), located at B8 hex of the SFR map								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics			PT2	PS0	PT1	PX1	PT0	PX0
Reset value	1	0	0	0	0	0	0	0

Table 16 Description of Interrupt Priority Register SFR IP

MNEMONIC	BIT POSITION	FUNCTION
	IP.7	not implemented, return a 1 when read.
	IP.6	not implemented.
PT2	IP.5	Define the priority of Timer2 overflow interrupt, or T2EX-pin (shared with P1.1) interrupt. When IP.5 = 1, Timer 2 overflow is a high priority interrupt. When IP.5 = 0, Timer 2 overflow is a low priority interrupt.
PS0	IP.4	Define the priority level of UART interrupt. When IP.4 = 1, UART interrupt is a high priority interrupt. When IP.4 = 0, UART interrupt is low priority interrupt.
PT1	IP.3	Define the interrupt level of Timer 1 overflow interrupt. When IP.3 = 1, Timer 1 overflow interrupt is a high priority interrupt. When IP.3 = 0, Timer 1 overflow interrupt is a low priority interrupt.
PX1	IP.2	Define the interrupt level of External Interrupt 1. When IP.2 = 1, External Interrupt 1 is a high priority interrupt. When IP.2 = 0, External Interrupt 1 is a low priority interrupt.
PT0	IP.1	Define the interrupt level of Timer 0 overflow interrupt. When IP.1 = 1, Timer 0 overflow is a high priority interrupt. When IP.1 = 0, Timer 0 overflow is a low priority interrupt.
PX0	IP.0	Define the interrupt level of External Interrupt 0. When IP.0 = 1, External Interrupt 0 is a high priority interrupt. When IP.1 = 0, External Interrupt 0 is a low priority level.

7.4 Interrupt Vectors

The vector indicates the Program Memory location where the appropriate interrupt service routine starts. Please refer to Table 12 for interrupt vector addresses.

8 OVERALL VIEW OF THE INTERRUPT SYSTEM

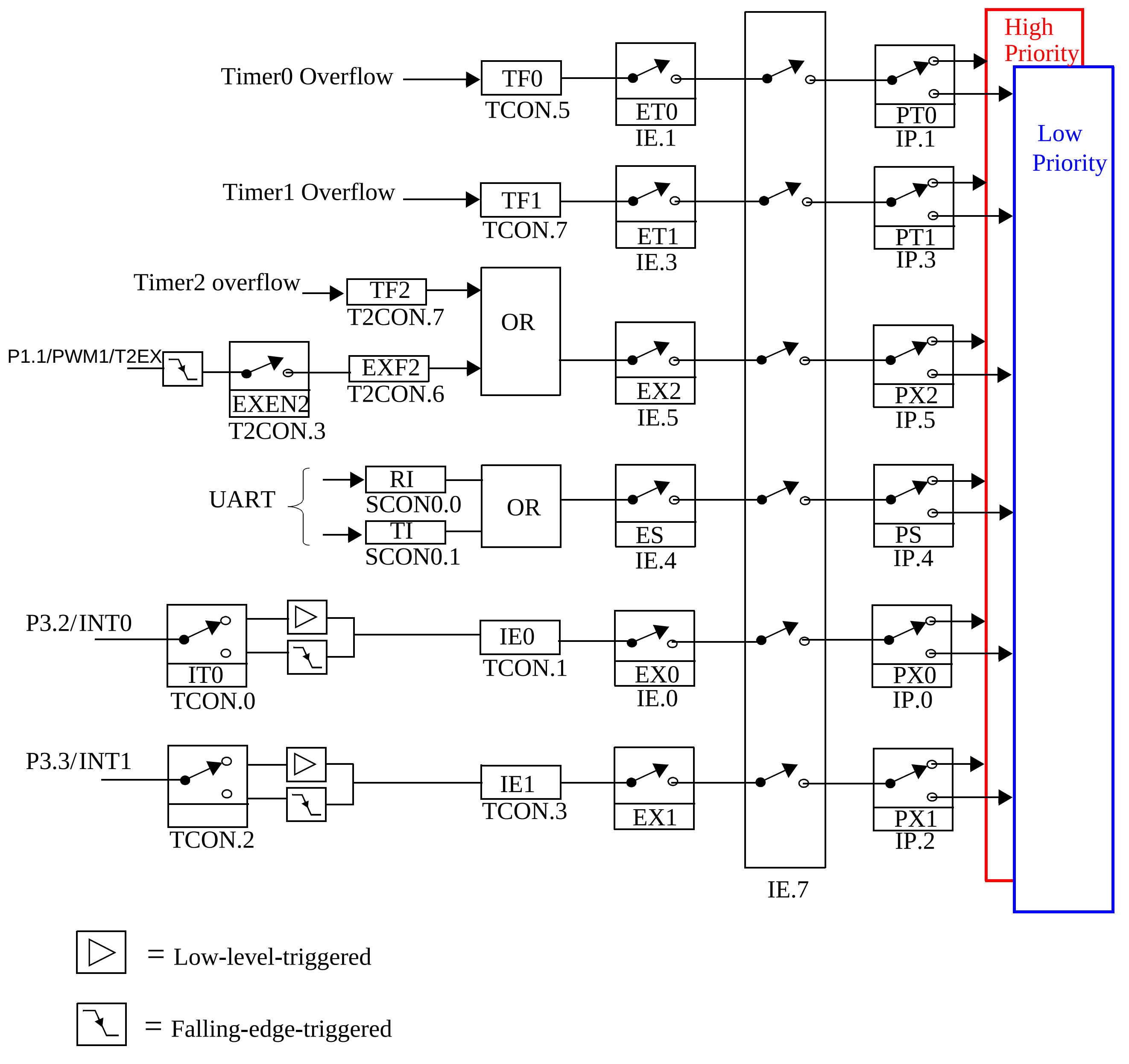


Fig.11 Overall view of interrupt system.

9 SPECIAL FUNCTION REGISTERS

The STK6031 has 47 Special Function Registers (SFR).

9.1 SFR Map Overview (47 SFRs)

Table 17 The SFR Map

Address (Hex)	R/W	SYMBOLS	DESCRIPTION	Reset Value
80	R/W	P0	Port 0 output latch (bit-addressable).	1111 1111
81	R/W	SP	Stack Pointer	0000 0111
82	R/W	DPL0	Data Pointer 0 Low (traditional 80C51 data pointer)	0000 0000
83	R/W	DPH0	Data Pointer 0 High (traditional 80C51 data pointer)	0000 0000
84	R/W	DPL1	Data Pointer 1 Low (extra data pointer), specific to the STK6031.	0000 0000
85	R/W	DPH1	Data Pointer 1 High (extra data pointer), specific to the STK6031.	0000 0000
86	R/W	DPS	DPTR Select Register (DPS), specific to the STK6031.	0000 0000
87	R/W	PCON	Power Control Register.	0011 0000
88	R/W	TCON	Timer0/1 Control Register (bit-addressable)	0000 0000
89	R/W	TMOD	Timer0/1 Mode Register	0000 0000
8A	R/W	TL0	Timer0, Low byte	0000 0000
8B	R/W	TL1	Timer1, Low byte	0000 0000
8C	R/W	TH0	Timer0, High byte	0000 0000
8D	R/W	TH1	Timer1, High byte	0000 0000
8E	R/W	CKCON	Clock Control register, specific to the STK6031. The register is for controlling the frequency of the clock added to Timer 0, Timer 1, and Timer 2, and memory stretch cycle for the MOVX instruction.	0000 0001
8F	not used.			
90	R/W	P1	Port 1 output latch (bit-addressable).	1111 1111
91, 92, 93, 94, 95, 96, 97, not used.				
98	R/W	SCON0	Serial Port Control/Status Register 0(bit-addressable)	0000 0000
99	R/W	SBUF0	Serial Port Buffer Register 0	0000 0000
9A, 9B, 9C, 9D, 9E, 9F not used				
A0	R/W	P2	Port 2 output latch (bit-addressable)	1111 1111
A1, A2, A3, A4, A5, A6, A7 not used.				
A8	R/W	IE	Interrupt Enable Register (bit-addressable)	0000 0000
A9, AA, AB, AC, AD, AE, AF not used.				
B0	R/W	P3	Port 3 output latch (bit-addressable)	1111 1111
B1, B2, B3, B4, B5, B6, B7, not used.				
B8	R/W	IP	Interrupt Priority Register (bit-addressable)	1000 0000
B9, BA, BB, BC, BD, BE, not used.				
BF	R/W	CHIPCON	Chip Configuration Register	xxx1 0000
C0	R/W	P4	Port 4 output latch.	1111 1111
C1, C2, C3, C4, C5, C6, C7, not used.				

Address (Hex)	**R/W**	**SYMBOLS**	**DESCRIPTION**	Reset Value
C8	R/W	T2CON	Timer 2 Control Register (bit-addressable)	0000 0000
C9	R/W	T2MOD	Timer 2 Mode Control Register	0000 xxx1x
CA	R/W	RCAP2L	Timer 2 Reload Capture Register, Low byte	0000 0000
CB	R/W	RCAP2H	Timer 2 Reload Capture Register, High byte	0000 0000
CC	R/W	TL2	Timer 2, Low byte	0000 0000
CD	R/W	TH2	Timer 2, High byte	0000 0000
CE, CF not used.				
D0	R/W	PSW	Program Status Word Register (bit-addressable)	0000 0000
D1	R/W	P1_OPT	Selecting Port 1 pin function, as normal port pin or PWM output.	xxx0 0000
D2	R/W	PWM0D	Pulse width modulation, channel 0	1000 0000
D3	R/W	PWM1D	Pulse width modulation, channel 1	1000 0000
D4	R/W	PWM2D	Pulse width modulation, channel 2	1000 0000
D5	R/W	PWM3D	Pulse width modulation, channel 3	1000 0000
D6	R/W	PWM4D	Pulse width modulation, channel 4	1000 0000
D7, D8 not used.				
D9	R/W	P4_OPT	Selecting Port 4 pin function, as normal port pin or ADC input.	
DA	R/W	ADCSE	Configuring P4.0 ~ P4.3 pins as ADC input pins.	0xxx 0000
DB	R	ADCVAL	Buffer for storing the converted digital value of the 6-bit ADC.	xx00 0000
DC, not used.				
DD		P0_OPT	Port 0 pin option for normal I/O or external memory address/data.	1111 1111
DE		P2_OPT	Port 2 pin option for normal I/O or external memory address.	1111 1111
DF not used				
E0	R/W	ACC	Accumulator (bit-addressable)	0000 0000
E1	R/W	WDT	Watchdog Timer Control.	00xx x000
E2	R/W	ISPSLV	ISP Control Slave address	0000 0000
E3	R/W	ISPEN	ISP Enable register (write 93hex to enable the ISP mode)	0000 0000
E4 ~EF not used.				
F0	R/W	B	B Register (bit-addressable)	0000 0000
F1 ~ FF not used.				

9.2 SFR of Each Functional Block

Table 18 SFR of each functional block

BLOCK	SYMBOL	NAME	Address (Hex format)	RESET VALUE
CPU	ACC	Accumulator.	E0	0000 0000
	B	B register	F0	0000 0000
	SP	Stack Pointer	81	0000 0111
	DPL0	Data Pointer 0, Low byte	82	0000 0000
	DPH0	Data Pointer 0, High byte	83	0000 0000
	DPL1	Data Pointer 1, Low byte	84	0000 0000
	DPH1	Data Pointer 1, High byte	85	0000 0000
	DPS	Selection for active Data Pointer	86	0000 0000
	PCON	Power Control Register	87	0011 0000
	PSW	Program Status Word	D0	0000 0000
	CHIPCON	Chip Configuration Register	BF	xxx1 0000
	CKCON	Clock Control Register	8E	0000 0001
Interrupt System	IE	Interrupt Enable Register	A8	0000 0000
	IP	Interrupt Priority Register	B8	x000 0000
Ports	P0	Port 0 latch	80	1111 1111
	P0_OPT	Port 0 pin option for I/O or external memory access	DD	1111 1111
	P1	Port 1 latch	90	1111 1111
	P1_OPT	Port 1 pin option for I/O or PWM outputs	D1	xxx0 0000
	P2	Port 2	A0	1111 1111
	P2_OPT	Port 2 pin option for I/O or external memory access	DE	1111 1111
	P3	Port 3 latch	B0	1111 1111
	P4	Port 4 latch	C0	xxxx 1111
	P4_OPT	Port 4 pin option for I/O or ADC inputs	D9	xxxx 0000
UART	SBUF0	Serial Port Buffer Register	99	???? ????
	SCON0	Serial Port Control/Status Register	98	0000 0000
Timer 0 / Time 1	TCON	Timer 0/1 Control Register	88	0000 0000
	TMOD	Timer 0/1 Mode Register	89	0000 0000
	TL0	Timer 0, Low byte	8A	0000 0000
	TL1	Timer 1, Low byte	8B	0000 0000
	TH0	Timer 0, High byte	8C	0000 0000
	TH1	Timer 1, High byte	8D	0000 0000
	CKCON	Clock Control Register	8E	0000 0001

BLOCK	**SYMBOL**	**NAME**	**Address (Hex format)**	**RESET VALUE**
Timer 2	T2CON	Timer 2 Control Register	C8	0000 0000
	T2MOD	Timer 2 Mode Control Register	C9	0000 xxx1x
	RCAP2L	Timer 2 Reload Capture Register, Low byte	CA	0000 0000
	RCAP2H	Timer 2 Reload Capture Register, High byte	CB	0000 0000
	TL2	Timer 2, Low byte	CC	0000 0000
	TH2	Timer 2, High byte	CD	0000 0000
	CKCON	Clock Control Register	8E	0000 0001
Watchdog Timer	WDT	Watchdog Timer Control Register	E1	00xx x000
PWM	P1_OTP	Port 1 pin selection for PWM outputs	D1	xxx0 0000
	PWM0D	PWM0 width	D2	1000 0000
	PWM1D	PWM1 width	D3	1000 0000
	PWM2D	PWM2 width	D4	1000 0000
	PWM3D	PWM3 width	D5	1000 0000
	PWM4D	PWM4 width	D6	1000 0000
ADC	P4_OPT	Select Port 4 pin function	D9	xxxx 0000
	ADCSEL	Select ADC input channel for conversion	DA	0xxx 0000
	ADCVAL	Buffer for converted ADC value.	DB	xx00 0000
ISP	ISPSLV	ISP Control slave address	E2	0000 0000
	ISPEN	Write 93 (hex) to enable the ISP mode	E3	0000 0000

10 TIMER/COUNTER 0, TIMER/COUNTER 1

10.1 General Description

There are seven SFRs associated with Timer/Counter 0 and Timer/Counter 1, as given in Table 19. Both Timer/Counter 0 and Timer/Counter 1 can be configured to operate either as timers or event counters.

Table 19 SFRs associated with Timer/Counter 0 and Timer/Counter 1.

SFR name	Address (hex) in SFR space	**Description**	Reset value (hex)
TL0	8A	These two SFRs are the lower 8 bits and higher 8 bits of Timer/Counter 0.	00
TH0	8C		00
TL1	8B	These two SFRs are the lower 8 bits and higher 8 bits of Timer/Counter 1.	00
TH1	8D		00
TCON	88	Control register for Timer/Counter 0 and Timer/Counter 1.	00
TMOD	89	Mode selection register for Timer/Counter 0 and Timer/Counter 1.	00
CKCON	8E	Clock frequency selection for Timer/Counter 0 and Timer/Counter 1.	01

Timer/Counter 0 and Timer/Counter 1 can be programmed to work in 4 operating modes:

- Mode 0: 13-bit timer/counter
- Mode 1: 16-bit timer/counter
- Mode 2: 8-bit counter with auto-reload
- Mode 3: Two 8-bit counters (only available from Timer 0)

10.2 Mode Selection Register, SFR TMOD (at 89H of SFR space)

MSB							LSB
Gate	$C/\overline{T}$	M1	M0	Gate	$C/\overline{T}$	M1	M0
Timer 1				Timer 0			

Table 20 Timer 0/1 Mode Selection Register

TIMER 0/1 MODE REGISTER (TMOD), LOCATED AT 89H OF THE SFR SPACE								
Bit Address	TMOD.7	TMOD.6	TMOD.5	TMOD.4	TMOD.3	TMOD.2	TMOD.1	TMOD.0
Mnemonics	Gate (Timer1)	$C/\overline{T}$ (Timer1)	M1 (Timer1)	M0 (Timer1)	Gate (Timer0)	$C/\overline{T}$ (Timer0)	M1 (Timer0)	M0 (Timer 0)

Table 21 Description of Timer 0/1 Mode Selection Register

MNEMONIC	BIT POSITION	FUNCTION
GATE	TMOD.7	Gating control for Timer 1. When set, Timer 1 is enabled only while INT1 pin is high and TR1 control bit is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
C/$\overline{T}$	TMOD.6	Timer or Counter selection of Timer 1. When set, counter operation is selected. When cleared, timer operation is selected.
M1, M0	TMOD.5 TMOD.4	Mode selection of Timer 1 • (M1, M0) = 00 selects Mode 0 operation. • (M1, M0) = 01 selects Mode 1 operation. • (M1, M0) = 10 selects Mode 2 operation. • (M1, M0) = 11 selects Mode 3 operation.(In mode 3, Timer/Counter 1 is stopped.)
GATE	TMOD.3	Gating control for Timer 0. When set, Timer 0 is enabled only while INT0 pin is high and TR0 control bit is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
C/T	TMOD.2	Timer or Counter selection of Timer 0. When set, counter operation is selected. When cleared, timer operation is selected.
M1, M0	TMOD.1, TMOD.0	Mode selection of Timer 0 • (M1, M0) = 00 selects Mode 0 operation. • (M1, M0) = 01 selects Mode 1 operation. • (M1, M0) = 10 selects Mode 2 operation. • (M1, M0) = 11 selects Mode 3 operation. (In mode 3, Timer/Counter 1 is stopped.)

10.3 Timer 0/1 Control Register (SFR TCON at 88 H of the SFR space)

Table 22 Timer 0/1 Control Register

TIMER 0/1 CONTROL REGISTER (TCON), LOCATED AT 88H OF THE SFR SPACE								
Bit Address	TCON.7	TCON.6	TCON.5	TCON.4	TCON.3	TCON.2	TCON.1	TCON.0
Mnemonics	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 23 Description of Timer 0/1 Control Register

MNEMONIC	BIT POSITION	FUNCTION
TF1	TCON.7	Timer 1 overflow flag. Set by hardware on Timer/Counter 1 overflow. Cleared by hardware when processor vectors to interrupt routine, or clearing the bit in software.
TR1	TCON.6	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
TF0	TCON.5	Timer 0 overflow flag. Set by hardware on Timer/Counter 0 overflow. Cleared by hardware when processor vectors to interrupt routine, or clearing the bit in software.
TR0	TCON.4	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
IE1	TCON.3	External Interrupt 1 Flag. Set by hardware when external interrupt 1 is detected. This bit is cleared after the interrupt is processed. That is, when the Return from Interrupt instruction is executed.
IT1	TCON.2	Interrupt 1 Type Control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.
IE0	TCON.1	External Interrupt 0 Flag. Set by hardware when external interrupt 0 is detected. This bit is cleared after the interrupt is processed. That is, when the Return from Interrupt instruction is executed.
IT0	TCON.0	Interrupt 0 Type Control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

10.4 Clock Control Register, SFR CKCON, at address 8E hex of the SFR map

For a description of the Clock Control Register, please refer to Table 3 and Table 4.

10.5 Operating Modes

10.5.1 MODE 0 (13-BIT TIMER/COUNTER)

When in mode 0, either of Timer 0 and Timer1 acts as a 13-bit counter. Fig.12 shows the operation of both Timer 0 and Timer 1 in mode 0 operation.

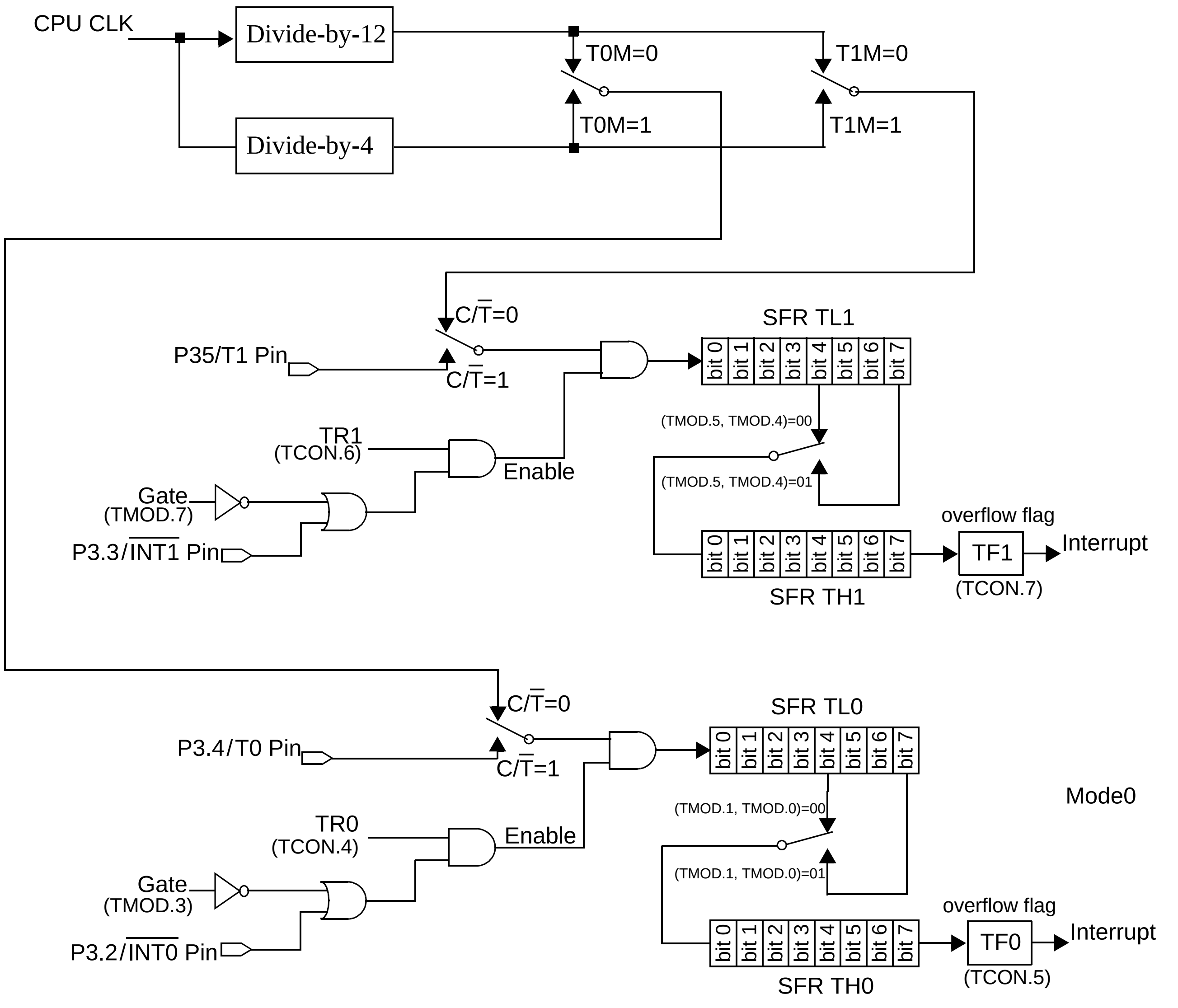


Fig.12 Mode 0 (13-bit timer/counter) and Mode 1 (16-bit timer/counter)

In this mode, the **Timer 0/Timer 1** registers are configured as a 13-bit register, which is composed of all the 8 bits of the TH1 (TH0) and the lower 5 bits of TL1 (TL0). The upper 3 bits of the TL1 (TL0) are indeterminate. The Timer Interrupt flag TF1 (TF0) is set to HIGH when the 13-bit register, acting as a counter, rolls over from all 1s to all 0s.

The 13-bit register (counter) is enabled only under the following conditions:

1. TR0 (TR1)=1, and
2. Either Gate=0 or $\overline{\text{INT1}}$ ($\overline{\text{INT0}}$)=1.

10.5.2 MODE 1 (16-BIT TIMER/COUNTER)

The configuration and operation of Mode 1 is the same as that of Mode 0, except that the registers are now 16 bits, instead of 13 bits when in Mode 0. Please refer to Fig.12.

10.5.3 MODE 2 (8-BIT COUNTER WITH AUTO-RELOAD)

Mode 2 configures the SFR TL0 and SFR TL1 as an 8-bit counter, respectively, with automatic reloading from SFR TH0 and SFR TH1, respectively. When the contents of TL1(TL0) changes from all 1s to all 0, the corresponding flags TF1 (TF0) is set to HIGH and the content of TH1(TH0) is reloaded into TL1 (TL0).The action of this reloading does not change the content TH1(TH0). The content of TH1 (TH0) can only be changed via programming these two SFRs.

As illustrated in Fig.12 and Fig.13, the control (enable) signal for mode 0, mode 1 and mode 2 are all the same.

Fig.13 shows the operation of Timer 0 and Timer 1 in mode 2.

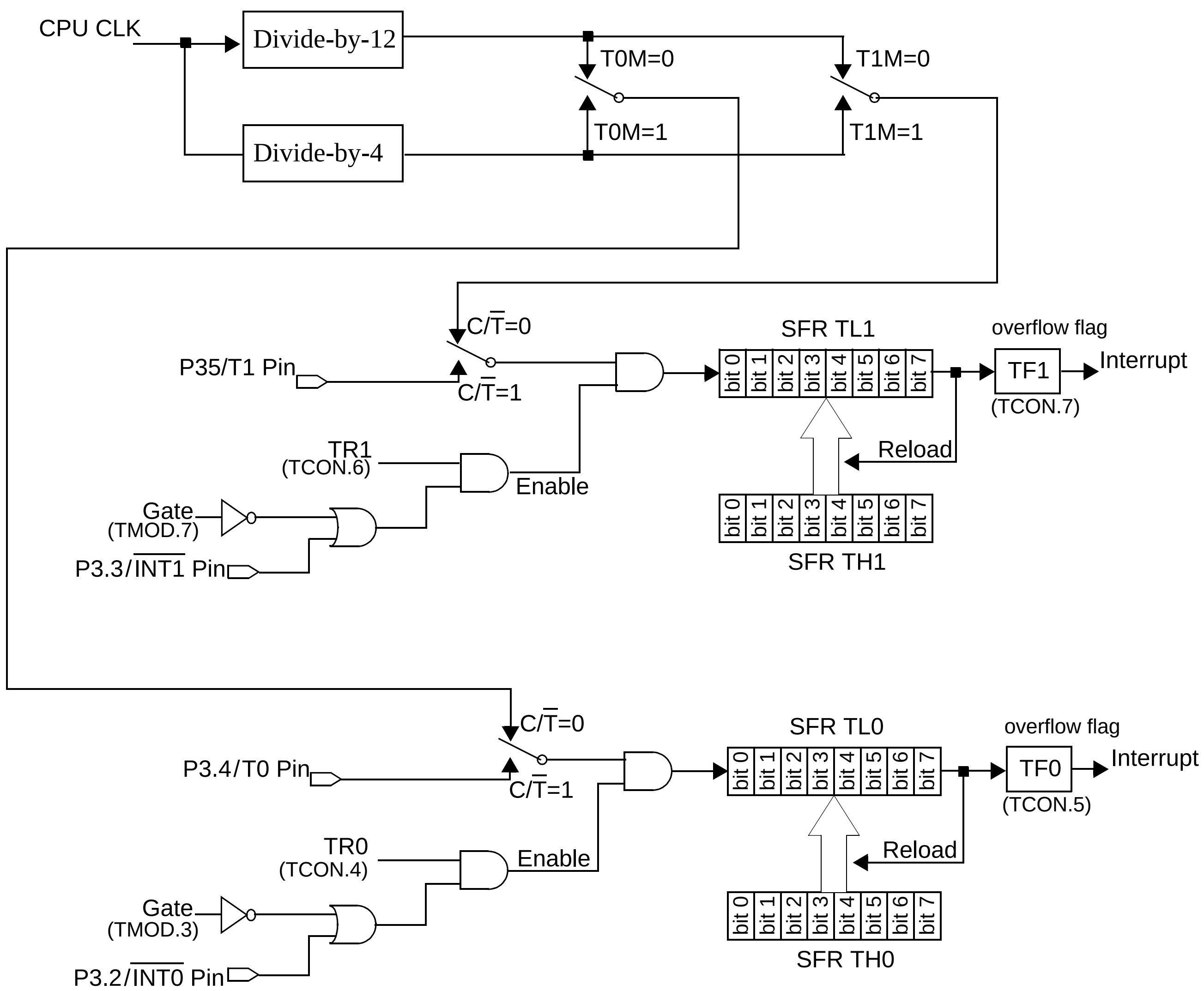


Fig.13 Mode 2 operation of Timer 0, Timer 1.

10.5.4 MODE 3 (TWO 8-BIT COUNTERS FROM TIMER 0)

When in Mode 3, Timer 1 stops counting and holds it value, and Timer 0 is configured into two separate counters: **TL0** and **TH0**. The logic of Timer 0 in Mode 3 is shown below.

TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is configured into a timer function (counting machines cycles) and takes over the use of TR1 and TF1 from Timer 1. Hence, TH0 now controls the Timer 1 interrupt.

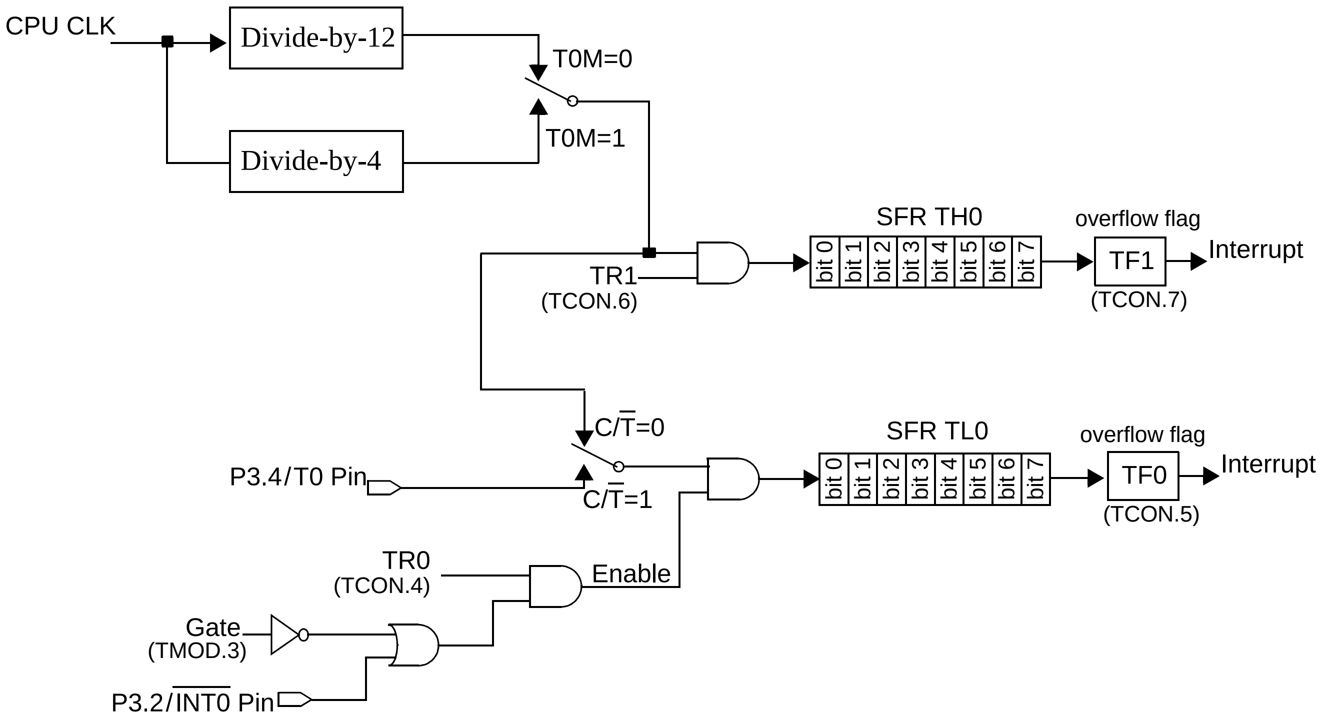


Fig.14 Mode 3 operation of Timer 0, Timer 1

11 TIMER/COUNTER 2

11.1 General Description and operation modes

Timer 2 is mainly composed of four SFRs, TH2, TL2, RCAP2L, RCAP2H, and their control logic.

SFR TH2 and SFR TL2 are cascaded into a 16-bit timer or counter, called Timer 2, which can be driven by either XTAL1 clock or off-chip clock pulse.

SFR RCAP2L and SFR RCAP2H are also cascaded into a 16-bit register. This register is used as a capture register or reload register. When used as a capture register, it can captures the content of Timer 2. When used as a reload register, it can reloads its content into Timer 2.

Timer 2's clock source can be from on-chip XTAL1 clock or off-chip clock pulse, depending on the state of the $C/\overline{T2}$ bit, bit 1 of SFR T2CON.

Timer 2 can operate in four different modes, listed below:

- 16-bit timer/counter,
- 16-bit timer/counter with capture,
- 16-bit timer/counter with auto-reload, or
- Baud-rate generator for UART.

Table 24 describes how to configure Timer T2 to operate in different operating modes.

Table 24 Configuring Timer 2 into various operating modes

RCLK (T2CON.5)	TCLK (T2CON.4)	$CP/\overline{RL2}$ (T2CON.0)	TR2 (T2CON.2)	OPERATING MODE
0	0	1	1	• 16-bit timer/counter, or • 16-bit timer/counter with capture capability.
0	0	0	1	16-bit timer/counter with auto-reload.
1	X	X	1	Baud rate generator for UART.
X	1	X	1	• Either RCLK=1 or TCLK=1 will configure Timer 2 into Baud Rate Generator mode. • When Timer 2 is in Baud Rate Generator Mode, bit $CP/\overline{RL2}$ is ignored.
X	X	X	0	When TR=1, clock pulses is blocked from entering into Timer 2. That is, Timer 2 is disabled.
X=don't care				

11.2 Special Function Registers associated with Timer 2

Timer 2 is associated with the 7 SFRs, listed in Table 25. Three SFRs, CKCON, T2CON, and T2MOD, must be properly programmed to have timer 2 work properly.

Table 25 Timer 2 SFRs

ADDRESS	R/W	MNEMONICS	DESCRIPTION	VALUE AFTER RESET
8E	R/W	CKCON	Select clock frequency for Timer 0, Timer 1, and Timer 2, and memory stretch cycle for the MOVX instruction.	0000 0000
C8	R/W	T2CON	Timer 2 Control Register (bit-addressable)	0000 0000
C9	R/W	T2MOD	Timer 2 Mode Control register	xxxx xx0x
CA	R/W	RCAP2L	Timer 2 Reload/Capture Register, Low byte	0000 0000
CB	R/W	RCAP2H	Timer 2 Reload/Capture Register, High byte	0000 0000
CC	R/W	TL2	Timer 2, Low byte	0000 0000
CD	R/W	TH2	Timer 2, High byte	0000 0000

11.2.1 THE T2M BIT OF CLOCK CONTROL REGISTER (SFR CKCON)

The T2M bit (bit 5) of the Clock Control Register (CKCON SFR), located at 8E(hex) of the SFR memory space, selects the frequency of the clock used to drive Timer 2.

When the T2M bit is programmed to LOW (T2M=0), (XTAL1÷12) clock is selected to drive Timer 2. When the T2M bit is programmed to HIGH (T2M=1), (XTAL1÷4) clock is selected to drive Timer 2. This bit has no effect when Timer 2 is programmed to work as a baud rate generator.

Table 26 T2M bit of SFR CKCON

Clock Control Register (SFR CKCON), located at 8E(hex) of the SFR map								
Bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonics	Reserved		T2M	T1M	T0M	MD2	MD1	MD0
Reset value	0	0	0	0	0	0	0	1

Table 27 Description of the T2M bit of SFR CKCON

MNEMONIC	BIT POSITION	FUNCTION
T2M	CKCON.5	Select Timer 2 clock frequency. When T2M=0, Timer 2 uses (XTAL1 / 12) as clock frequency. When T2M=1, Timer 2 uses (XTAL1 / 4) as clock frequency.

For detailed description of the SFR CKCON, please refer to Table 9.

11.2.2 Timer 2 Control Register (SFR T2CON)

Table 28 and Table 29 give description for SFR T2CON.

Table 28 Timer 2 Control Register (SFR T2CON, C8 hex)

Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Reset Value	0	0	0	0	0	0	0	0

Table 29 Description of Timer 2 Control Register

MNEMONIC	BIT POSITION	FUNCTION
TF2	T2CON.7	Timer 2 overflow flag. • This bit is set to HIGH when Timer 2 overflows from FFFF(hex) to 0000(hex). It must be cleared by software. • TF2 will not be set when either RCLK or TCLK is 1. That is, when Timer 2 is in Baud Rate Generator mode, TF2 will never be set. • Writing a 1 to TF2 bit forces a Timer 2 interrupt, if this interrupt function is enabled.
EXF2	T2CON.6	Timer 2 External flag. • This bit is set to HIGH when a capture or reload action is triggered by a high-to-low transition on the T2EX input pin and when EXEN2=1. • When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to jump to Timer 2 interrupt subroutine. It must be cleared by software. • Writing a 1 to the EXF2 bit forces a Timer 2 interrupt, if it is enabled.
RCLK	T2CON.5	UART Receiver clock selection. This bit is used to select the receiver clock of the UART. • If this bit is programmed to 1 (RCLK=1), UART uses Timer 2 overflow pulses as its receiver clock in Modes 1 and 3. • If this bit is programmed to 0 (RCLK=0) , UART uses Timer 1 overflow pulses as its receiver clock.
TCLK	T2CON.4	UART Transmitter clock selection. This bit is used to select the transmitter clock of the UART. • If this bit is programmed to 1 (TCLK=1), UART uses Timer 2 overflow pulses as its transmitter clock in Modes 1 and 3. • If this bit is programmed to 1 (TCLK=0) , UART uses Timer 1 overflow pulses as its transmitter clock.
EXEN2	T2CON.3	Timer 2 external enable. • EXEN2=1 allows a capture or reload to occur as a result of a high-to-low transition on the T2EX input, if Timer 2 is not in baud rate generator mode. • EXEN2=0 causes Timer 2 to ignore all events at T2EX input.

MNEMONIC	BIT POSITION	FUNCTION
TR2	T2CON.2	Start/Stop control for Timer 2. • TR2=1 allows clocks to be added to Timer 2. • TR2=0 prevent clocks from being added to Timer 2.
$C/\overline{T2}$	T2CON.1	Select <u>timer function</u> or <u>counter function</u> of Timer 2. • $C/\overline{T2}$= 0 selects the timer function. • When used as a timer, Timer 2 runs at four XTAL1 clocks per increment or twelve XTAL1 clocks per increment, as selected by the T2M bit (CKCON.5) of the SFR CKCON, in all modes except baud rate generator mode. • When used in baud rate generator mode, Timer 2 runs at two XTAL1 per increment, independent of the state of the T2M bit. • $C/\overline{T2}$=1 selects the external event counter function; falling-edge-triggered on the T2 input.
$CP/\overline{RL2}$	T2CON.0	Selection of capture or reload function. • When this bit is programmed to HIGH ($CP/\overline{RL2}$ =1), Timer 2 is in capture mode and capture occurs on a high-to-low transitions (falling edge) at T2EX, if EXEN2=1. • When this bit is programmed to LOW ($CP/\overline{RL2}$ =0), Timer 2 is in auto-reload mode and auto-reload occurs either with Timer 2 overflows or a high-to-low transitions at T2EX when EXEN2=1. • When RCLK=1 or TCLK=1, this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

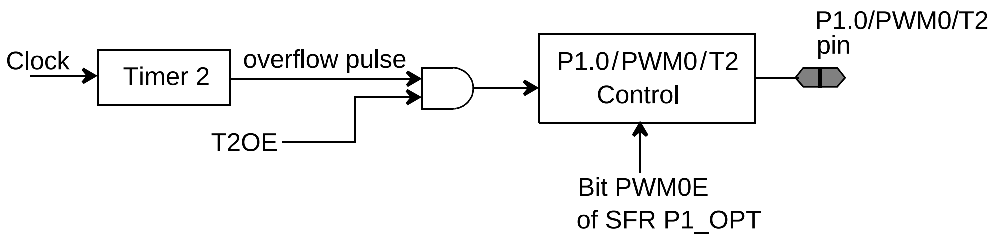
11.2.3 TIMER 2 MODE CONTROL REGISTER

Timer 2 Mode Control Register, located at C9(hex) of the SFR memory space, is a one-bit SFR. It is used to turn on Timer 2 pulse output to the P1.0/PWM0/T2 pin, when Timer 2 overflows from FFFFH.

Table 30 Timer 2 Mode Control Register (SFR T2MOD)

Timer 2 Control Register (SFR T2CON), located at C8(hex) of the SFR memory space.								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics							T2OE	
Reset Value	X	X	X	X	X	X	0	X

Table 31 Description of Timer 2 Control Register

MNEMONIC	BIT POSITION	FUNCTION
T2OE	T2MOD.1	Timer 2 output enable bit. Programming this bit to HIGH (T2OE=1) enables Timer 2 overflow pulse to be sent to the P1.0/PWM0/T2 pin, as illustrated in the following figure.  Fig.15 T2OE bit

11.3 16-bit Timer/Counter Mode

In this mode, SFR TL2 and SFR TH2 are cascaded into a 16-bit timer or counter. SFR RCAP2L and SFR RCAP2H are not used. This 16-bit timer can then be used to count pulses from on-chip XTAL1 clock or off-chip external pulses, by properly programming bits T2M and C/$\overline{T2}$. The TR2 bit, Timer 2 enable bit, must always be HIGH.

When Timer 2 overflows from FFFFH to 0000H, a clock pulse with the duration of one cycle of XTAL1 clock is sent out.This pulse then sets the Timer 2 overflow flag, which, if enabled, can generate an interrupt. The overflow pulse can also be sent to Pin1.0, if the T2OE bit is enabled.

Fig.17 shows Timer 2 configuration when it works as a 16-bit Timer/Counter.

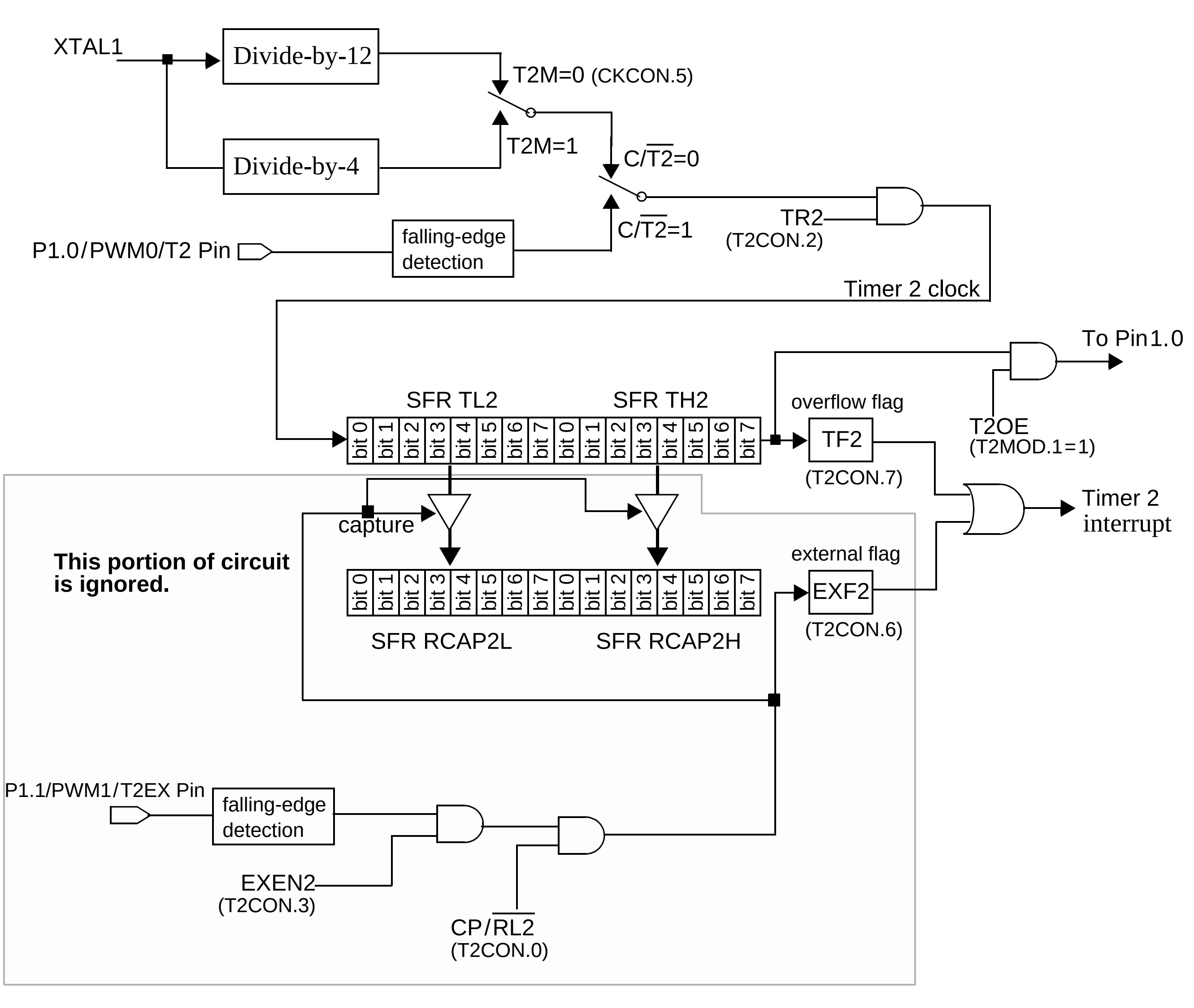


Fig.16 Timer 2 configuration in 16-bit timer/counter mode

11.4 16-bit Timer/Counter with Capture capability (Capture Mode)

When Timer 2 works in this mode, the content of SFR TL2 and SFR T2H can be captured into SFR RCAP2L and SFR RCAP2H, respectively, by an external triggering on the T2EX pin. Therefore, this mode is called Capture Mode.

Bit EXEN2 is used to enable external trigger.

- If EXEN2=0, external trigger is disabled and Timer 2 is a pure 16-bit timer/counter which, upon overflowing, sets the Timer 2 overflow flag bit TF2. This flag may then be used to generate an interrupt.
- If EXEN2=1, Timer 2 also operates as a 16-bit timer/counter, but with the additional capability that a **High-to-Low transition** at the T2EX input causes the current value in TL2 and TH2 to be captured into SFR RCAP2L and SFR RCAP2H. The falling transition at T2EX also causes the EXF2 flag bit in T2CON to be set; this flag may also be used to generate an interrupt. The triggering pulse is also conditioned by the CP/$\overline{\text{RL2}}$ bit. To enable the capture action, The CP/$\overline{\text{RL2}}$ bit must be set to HIGH.

In addition, Timer2 overflow pulse, whose duration is one cycle of Timer 2 clock, can be sent out to Pin 1.0, if T2OE=1.

Fig.17 shows Timer 2, working as a 16-bit Timer/Counter with Capture capability.

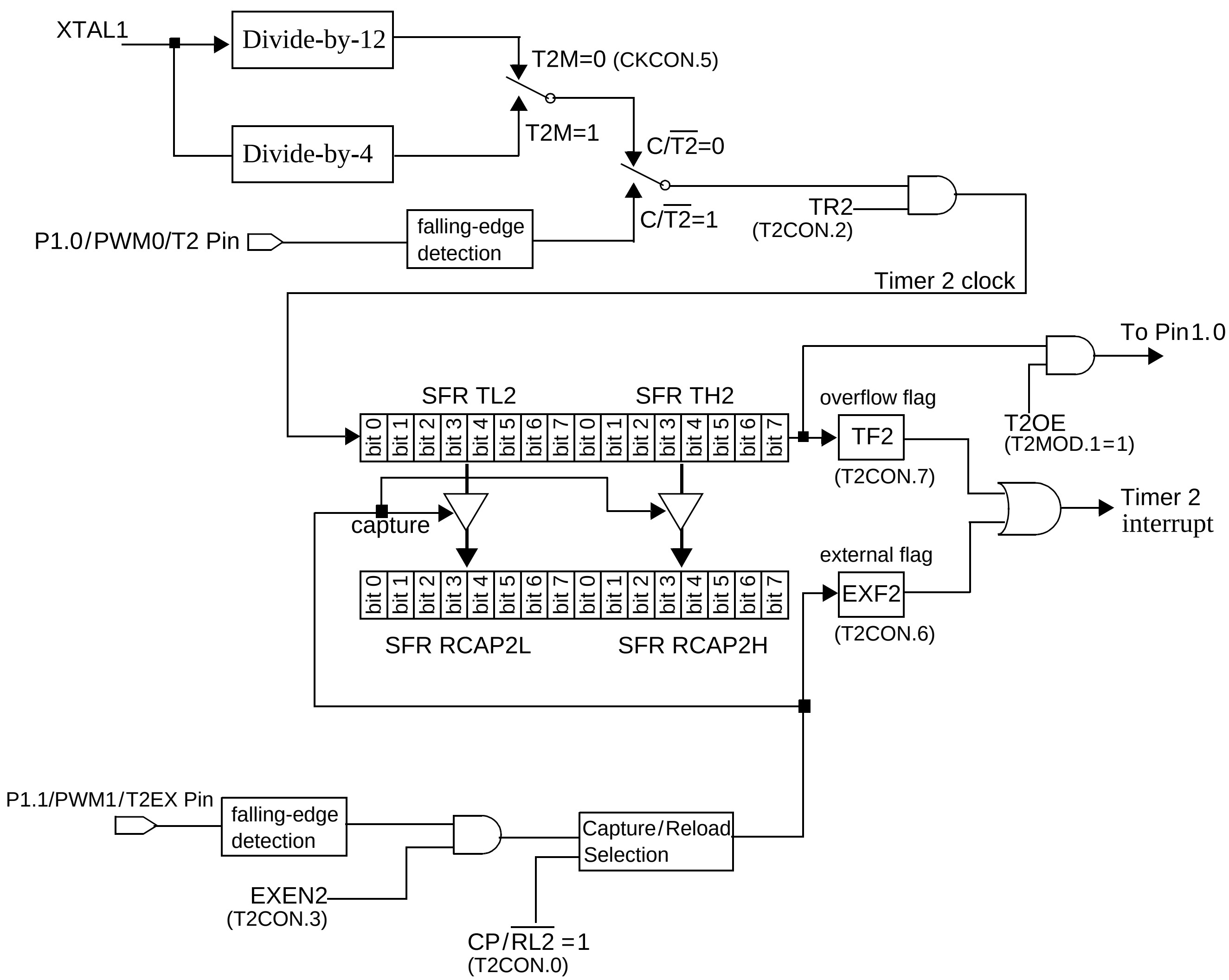


Fig.17 Timer 2 in 16-bit timer/counter mode with capture capability

11.5 16-bit Timer/Counter with Auto-Reload capability (Auto-Reload Mode)

When CP/$\overline{RL2}$=0, Timer 2 is configured into Auto-reload mode. In the Auto-Reload mode, the Timer 2's starting value is reloaded from SFR RCAP2L and SFR RCAP2H.

There are two options selected by the EXEN2 bit in T2CON.

- If EXEN2=0, then, when Timer 2 overflows from FFFFH, it sets the TF2 flag bit and also causes the Timer 2 registers to be reloaded with the 16-bit value held in SFR RCAP2L and SFR RCAP2H. The 16-bit value held in RCAP2L and RCAP2H should be pre-loaded by software.
- If EXEN2= 1, Timer 2 operates as described above, but with the additional feature that a High-to-Low transition at the external input pin T2EX will also trigger the16-bit reload and set the EXF2 flag bit.

In this mode, Timer 2 overflow pulse can also be sent to the P1.0 pin by setting the T2OE bit.

Fig.18 shows Timer 2 configuration in Auto-reload mode.

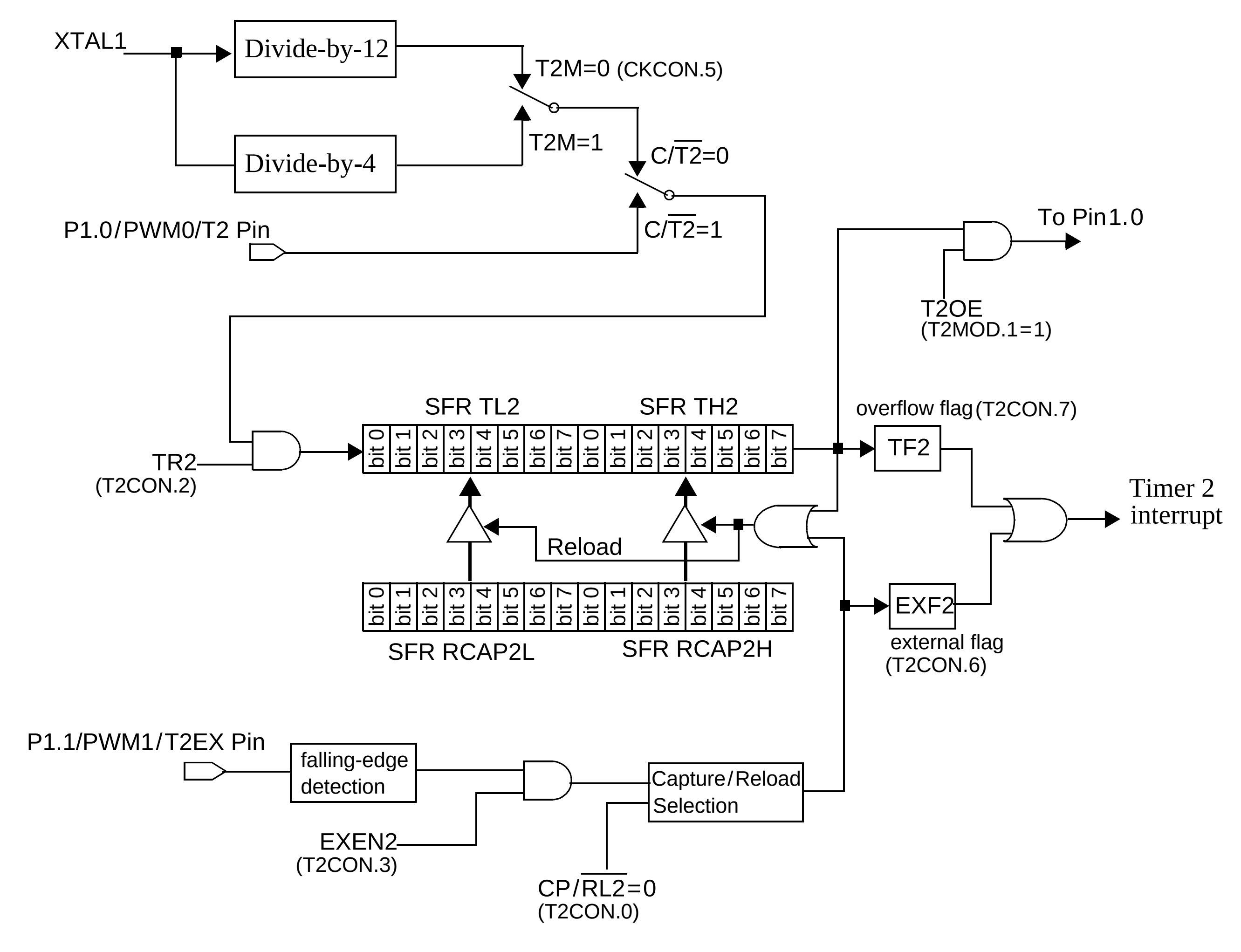


Fig.18 Timer 2 in auto-reload mode

11.6 Baud Rate Generator Mode

When either RCLK=1 or TCLK=1, Timer 2 is a baud rate generator for UART, without regard to the setting of CP/$\overline{\text{RL}}$2 bit. The overflow pulse from Timer 2, after being divided by a divided-by-16 counter, is used as the transmitting clock or receiving clock of the UART in Mode 1 or Mode 3.

The Baud Rate Generator mode is similar to the Auto-Reload mode, in that an overflow of Timer 2 causes Timer 2 registers (SFR TH2 and SFR TL2) to be reloaded with the 16-bit value held in the registers SFR RCAP2H and SFR RCAP2L, which should be preloaded by software.

As a baud rate generator, Timer 2 counts at a frequency of 1/2 f_{xtal1}, as shown in Fig.19.

Baud rates of the UART in Modes 1 and 3 are determined by the following equation.

$$\text{Baud Rate} = \frac{\text{Timer 2 overflow rate}}{16} = \frac{f(XTAL1)}{(32)\times[65536-(RCAP2H;RCAP2L)]} \text{ - - - - - - - Equation (1)}$$

In the above equation, (RCAP2H ; RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer. The 32 in the denominator is the result of the XTAL1 clock being divided by 2 and the Timer 2 overflow rate being divided by 16. Setting TCLK=1 or RCLK=1 automatically causes the XTAL1 clock to be divided 2.

11.6.1 CALCULATING THE VALUE OF RCAP2H AND RCAP2L FOR A DESIRED BAUD RATE

If a programmer has decided to use a certain baud rate, the required value of RCAP2H and RCAP2L and be derived from Equation (2), which is re-manipulated from the Equation (1).

$$(RCAP2H, RCAP2L) = 65536 - \frac{XTAL1}{32\times \text{Baudrate}} \text{ - - - - - - - Equation (2)}$$

Table 32 gives calculated value of RCAP2H and RCAP2L for some desired baud rates.

Table 32 Timer 2 reload value for UART Mode 1 and Mode 3 baud rate.

BAUD RATE	C/$\overline{\text{T2}}$	33 MHz XTAL1		25 MHz XTAL1		11.0592 MHz XTAL1	
		RCAP2H	RCAP2L	RCAP2H	RCAP2L	RCAP2H	RCAP2L
57.6 Kb/s	0	FF	EE	FF	F2	FF	FA
19.2 Kb/s	0	FF	CA	FF	D7	FF	EE
9.6 Kb/s	0	FF	95	FF	AF	FF	DC
4.8 Kb/s	0	FF	29	FF	5D	FF	B8
2.4 Kb/s	0	FE	52	FE	BB	FF	70
1.2 Kb/s	0	FC	A5	FD	75	FE	E0

11.6.2 More about Timer 2

When either RCLK or TCLK is set to logic high, Timer 2 overflow does not set the TF2 bit of SFR T2CON and therefore will not generate interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the baud rate generator mode.

If EXEN2 is set to HIGH, a HIGH-to-LOW transition on T2EX will set the EXF2 bit of T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2; TL2). Therefore, in this mode T2EX may still be used as an additional external interrupt.

When Timer 2 is operating in the baud rate generator mode, registers SFR TH2 and SFR TL2 should not be accessed. Because in this mode, the timer is being incremented every two XTAL1 clock and therefore the results of a read or write may not be accurate. The SFRs RCAP2H and RCAP2L, however, may be read out but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required, Timer 2 should first be turned off by clearing the TR2 bit.

11.6.3 Timer 2 in baud rate generator mode

The configuration of Timer 2 in baud rate generator mode is shown in Fig.19.

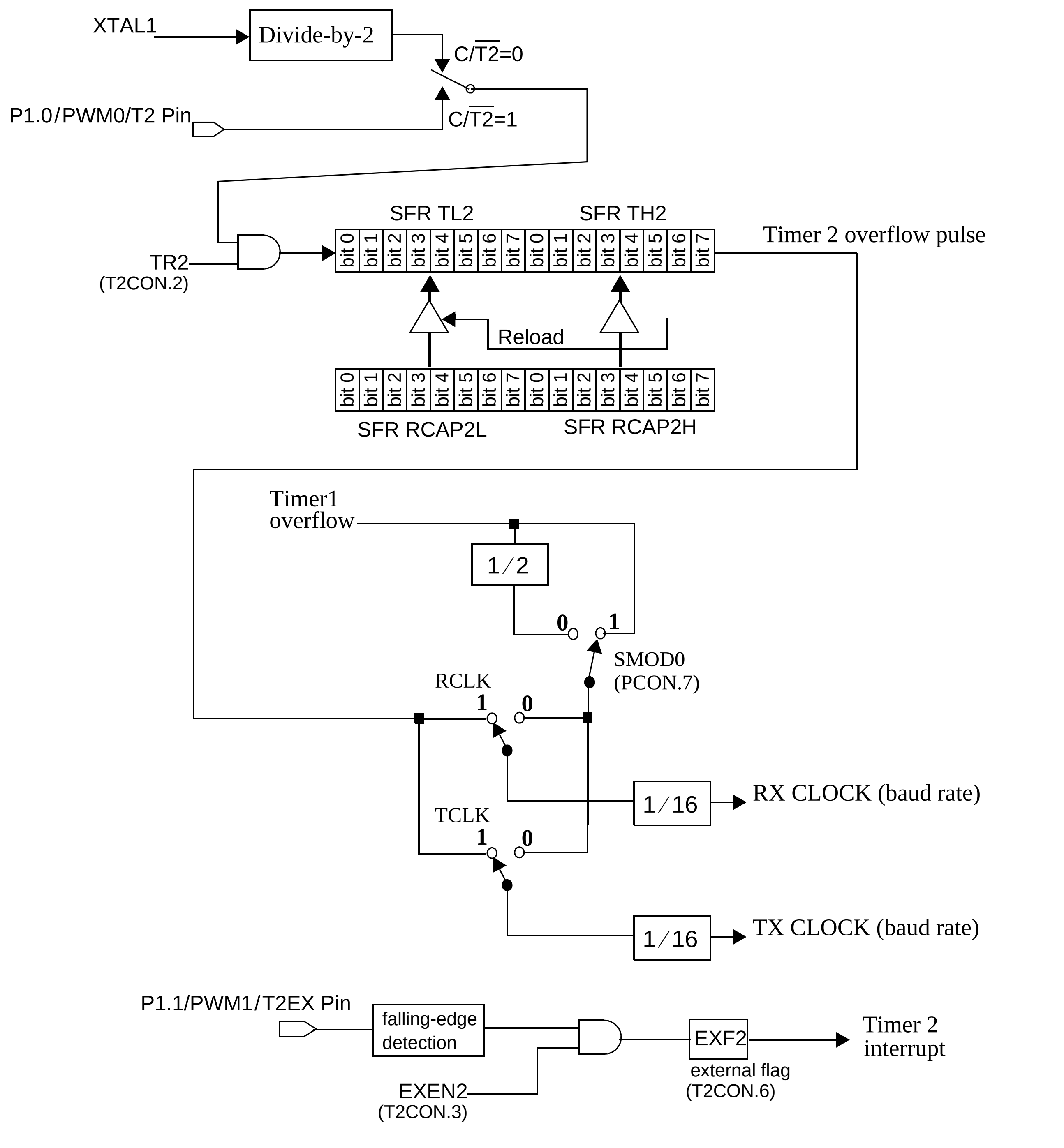


Fig.19 Timer 2 in baud-rate generator mode

12 UART0

12.1 General Description

The UART0 (Universal Asynchronous Receiver/Transmitter) is a full-duplex serial port. The word "full-duplex" means that it can transmit and receive simultaneously. It has one receiver data pin (RXD) and one transmitter data pin (TXD). The receiver data pin shares with port pin P3.0 and the transmitter data pin shares with port pin P3.1.

Two SFRs, SFR SCON0 and SFR SBUF0, are associated with the UART0.

- SFR SCON0, at 98H of the SFR memory space, is the control and status register of the UART0.
- SFR SBUF0, at 99H of the SFR memory space, is the data buffer for both transmission and reception.

From software point of view, data transmission and reception are both through the SFR SBUF0. Writing to SFR SBUF0 loads data to be transmitted to SFR SBUF0. Reading SFR SBUF0 reads received data.

But, physically, writing to SFR SBUF0 loads data to a physical Transmit Register and reading SFR SBUF0 reads a physical Receive Register.

A programmer's model of the UART0 is shown in Fig.20.

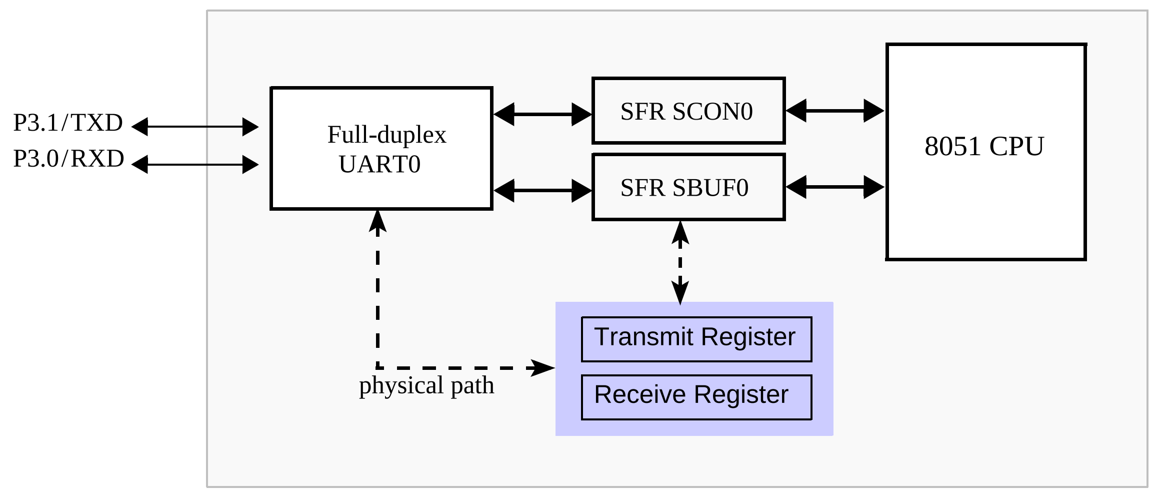


Fig.20 Programmer's model of the UART0

12.2 Operation modes

UART0 has 4 operation modes:

- Mode 0: 8-bit shift register,
- Mode 1: 10-bit data transmission/reception,
- Mode 2: 11-bit data transmission/reception, and
- Mode 3: 11-bit data transmission/reception.

Table 33 gives detailed description for each of the four operation modes.

The selection of operation modes depends on the setting of the SM0 bit and the SM1 bit of SFR SCON0.

Table 33 UART0 Operation Modes.

Mode	SM0	SM1	Description
Mode 0	0	0	**8-bit serial transmission or reception.** In this mode, 8 bits of data enters or exits through the P3.0/RXD pin. The P3.1/TxD pin always outputs the shift clock. The Least Significant Bit (LSB) is received or transmitted first. The baud rate is either 1/4 or 1/12 of the XTAL1 frequency.
Mode 1	0	1	**10-bit serial transmission or reception.** In this mode, 10 binary bits are transmitted (through P3.1/TXD) or received (through P3.0/RXD). The 10 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), and a **stop bit**(1). On reception, the stop bit goes into bit RB8 of the SFR SCON0. The baud rate comes from Timer 1 or Timer 2 overflow.
Mode 2	1	0	**11-bit serial transmission or reception.** In this mode, 11 binary bits are transmitted (through P3.1/TXD) or received (through P3.0/RXD). The 11 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), a programmable 9th data bit, and a **stop bit**(1). On transmission, the 9th data bit (TB8 in SCON0) can be programmed to be 1 or 0. For example, in application, the **parity bit P** of SFR PSW can be moved into TB8 of SCON0. On reception, the 9th data bit goes into RB8 of SFR SCON0, while the **stop bit** is ignored. The baud rate is programmable to be 1/32 or 1/64 of XTAL1 frequency.
Mode 3	1	1	**11-bit serial transmission or reception.** In this mode, 11 binary bits are transmitted (through P3.1/TXD) or received (through P3.0/RXD). The 11 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), a programmable 9th data bit, and a **stop bit**(1). Actually, Mode 3 is a combination of Mode 2 protocol and Mode 1 baud rate. The baud rate in Mode 3 comes from Timer 1 or Timer 2 overflow.

12.3 Serial Port Control/Status Register (SFR SCON0)

The Serial Port Control/Status Register is SFR SCON0, located at address 98H of the SFR memory space.

Table 34 Serial Port Control and Status Register (SFR SCON0, 98h)

Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	SM0	SM1	SM2	REN0	TB8	RB8	TI0	RI0

Table 35 Description of SFR SCON0

<table>
<tr><th>Mnemonic</th><th>Bit position</th><th>Function</th></tr>
<tr><td>SM0</td><td>SCON0.7</td><td rowspan="2">These two bits are used to select an operation mode.
<table><tr><th>SM0</th><th>SM1</th><th>Modes</th></tr><tr><td>0</td><td>0</td><td>Mode 0</td></tr><tr><td>0</td><td>1</td><td>Mode 1</td></tr><tr><td>1</td><td>0</td><td>M0de 2</td></tr><tr><td>1</td><td>1</td><td>Mode 3</td></tr></table></td></tr>
<tr><td>SM1</td><td>SCON0.6</td></tr>
<tr><td>SM2</td><td>SCON0.5</td><td>Multiprocessor Communication Enable.
In Mode 0, SM2 decides the baud rate. When SM2 = 0, the baud rate is $f_{xtal1}/12$. When SM2 = 1, the baud rate is $f_{xtal1}/4$.
In Mode 1:
• if SM2=1, then RI0 will be set to high only when a HIGH stop bit has been received.
• if SM2=0, then RI0 will always be set to high without regard to the state of the received stop bit.
In modes 2 and 3, SM2 enables the multiprocessor communication feature. SM2 is used to disable interrupt to the un-addressed slave receivers, when data bytes are transmitted from the master.</td></tr>
<tr><td>REN0</td><td>SCON0.4</td><td>Reception Enable.
When REN0=1, UART0 is enabled for reception.
When REN0=0, UART0 is disabled from reception.</td></tr>
<tr><td>TB8</td><td>SCON0.3</td><td>TB8 is the 9th data bit that will be transmitted in Mode 2 or Mode 3. Set or cleared by software as desired.</td></tr>
<tr><td>RB8</td><td>SCON0.2</td><td>In Mode 2 and Mode 3, RB8 is the 9th data bit received.
In Mode 1, RB8 indicates the state of the received stop bit.
In Mode 0, RB8 is not used.</td></tr>
<tr><td>TI0</td><td>SCON0.1</td><td>The Transmit Interrupt Flag. This flag can only be cleared by software.
In mode 0, this bit is set to a logic 1 by hardware at the end of the 8th bit time.
In mode 1, mode 2, and mode 3, this bit is set to a logic 1 by hardware at the beginning of the stop bit time.</td></tr>
<tr><td>RI0</td><td>SCON0.0</td><td>The Receive Interrupt Flag. This flag can only be cleared by software.
In mode 0, this bit is set to a logic 1 by hardware at the end of the 8th bit time.
In mode 1, this bit is set to logic 1 after the last sampling of the stop bit, subject to the state of SM2.
In mode 2, and mode 3, this bit is set to a logic 1 by hardware at the last sampling of the stop bit.</td></tr>
</table>

12.4 Mode 0

12.4.1 TRANSMISSION AND RECEPTION OF MODE 0

When operating in mode 0, the UART0 is an 8-bit data shift register. Eight bits of data can be shifted into or out from SFR SBUF0, via the P3.0/RXD pin. The shifting clock always comes out from the P3.1/TXD pin, without regard to if the data is shifted into or out from SFR SBUF0.

12.4.2 BAUD RATE OF MODE 0

In mode 0, the UART0's baud rate is either $f_{xtal1}/12$ or $f_{xtal1}/4$, depending on the value of the SM2 bit. If SM2 = 1, the baud rate (i.e., shifting clock frequency) is $f_{xtal1}/4$. If SM2 = 0, then the baud rate is $f_{xtal1}/12$.

12.4.3 TRANSMISSION TIMING OF MODE 0

Data transmission begins when an instruction writes to SFR SBUF0. That is, whenever an instruction with SFR SBUF0 as its destination operand is executed, data transmission will be initiated. The UART0 shifts the data out, LSB first, at the selected baud rate, until all 8 bits of data have been shifted out.

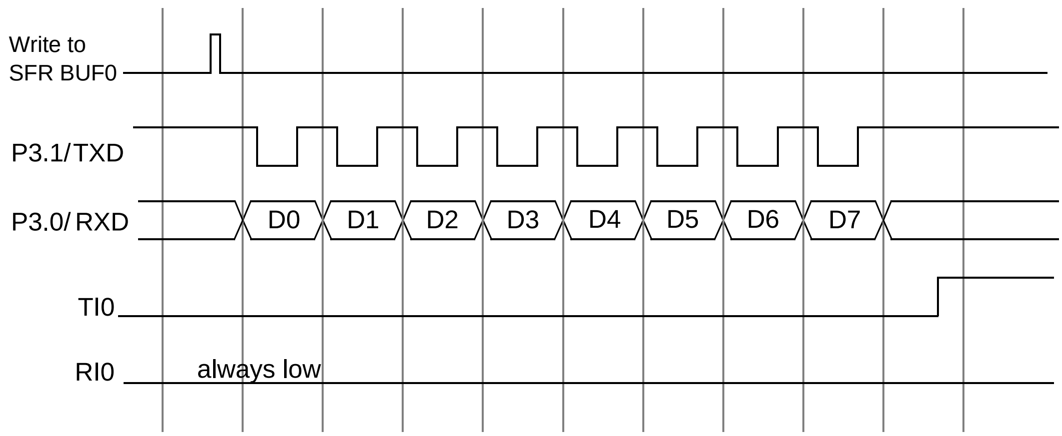


Fig.21 UART0 mode 0 transmission timing when baud rate is XTAL1/4.

12.4.4 RECEPTION TIMING OF MODE 0

To enable data reception, the REN0 bit must first be set to logic HIGH. Data reception begins when the RI0 bit is cleared. Shifting clock is then sent out from the P3.1/TXD pin to shift in data, LSB first, until all 8 bits of external data have been shifted in. Each bit of data is shifted in on the rising edge of the shifting clock. Four XTAL1 clocks after the 8th data bit has been shifted in, the RI0 bit is set to logic HIGH. The RI0=1 indicates that 8 bits of data have been received.

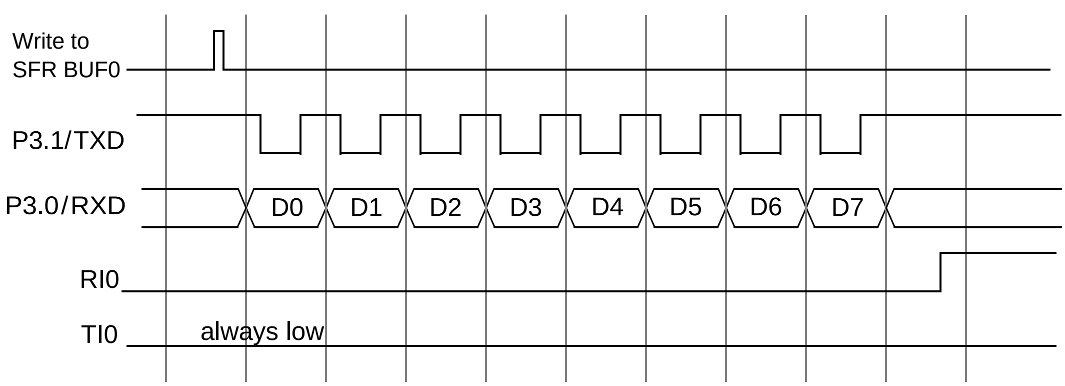


Fig.22 UART0 mode 0 reception timing when baud rate is XTAL1/4.

12.5 Mode 1

12.5.1 OPERATION OF MODE 1

Mode 1 provides 10-bits, asynchronous, full-duplex transmission or reception. One transmission or reception word is composed of the following bits:

- one start bit,
- eight data bits (D0~D7), and
- one stop bit.

The 10-bits word format is shown below:

START	D0	D1	D2	D3	D4	D5	D6	D7	STOP

The data bits are transmitted and received LSB first.

For receive operations, the received stop bit is stored to the RB8 bit of SFR SCON0.

12.5.2 BAUD RATE OF MODE 1

Mode 1 baud rate can be from timer 1 overflow or timer 2 overflow.

Please refer to Section 12.8 “Baud Rate Generation for Mode 1 and Mode 3”

12.5.3 DATA TRANSMISSION TIMING IN MODE 1

A data transmission session in mode 1 involve two steps:

1. Application program issues a write to SFR SBUF0,
2. Transmission begins immediately after the first overflow of the divided-by-16 counter of the Baud Rate Generation circuit (please refer to Fig.27).
3. The UART0 transmits data out from the P3.1/TXD pin in the following order: START bit, data bits (D0~D7), and STOP bit. The START bit is transmitted out first. The TI0 (SCON0.1) bit of SFR SCON0 is set to HIGH two XTAL1 clocks after the stop bit has been transmitted.

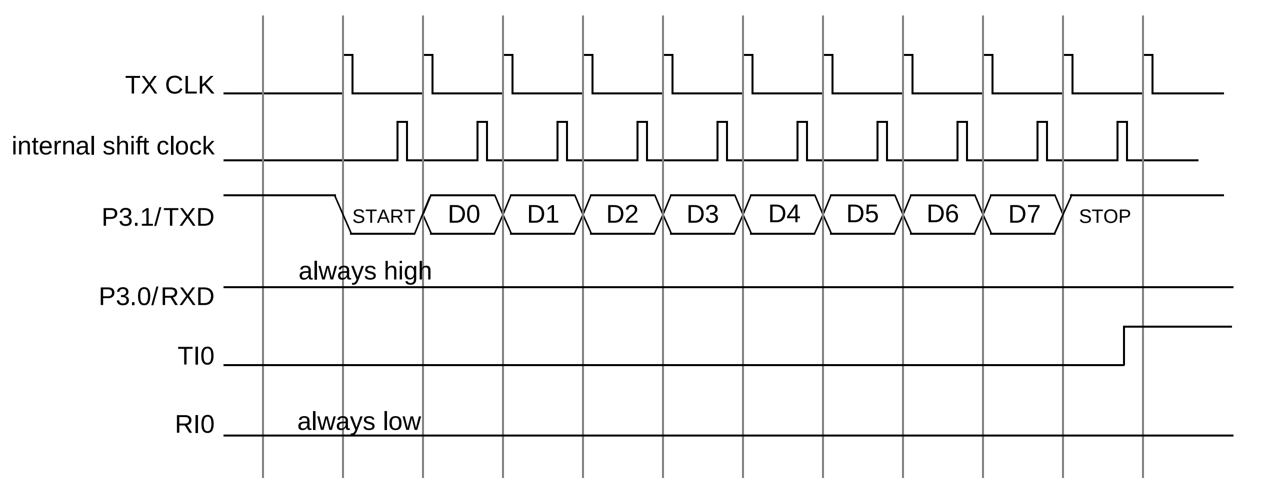


Fig.23 UART0 mode 1 transmission timing

12.5.4 DATA RECEPTION TIMING IN MODE 1

A data reception session in mode 1 is as follows:

1. First, the reception function of the UART0 must be enabled by setting REN0=1 and then the UART0 starts detecting if there is a falling edge on the P3.0/RXD input. For detecting this falling edge, UART0 samples the P3.0/RXD input pin sixteen times per bit time for any baud rate.
2. When a falling edge on the P3.0/RXD pin is detected, the divided-by-16 counter of the baud rate generation circuit is reset. The output of the divided-by-16 counter is the receiver clock, RX CLK. This action is for aligning Timer 1 or Timer 2 overflow to bit boundaries. Please refer to Fig.27 for baud rate generation circuit.
3. For noise rejection, the UART0 decides the value of each received bit by *majority decision* of three consecutive samples in the middle of each bit time. That is, if three consecutive sampled values are 110, then the received bit value is regarded as HIGH. Similarly, if three consecutive sampled values are 101, then the received bit value is still regarded as HIGH.
4. If the first received bit is not LOW, then the reception session is aborted and the UART0 waits for another falling edge on the P3.0/RXD pin.
5. If the first received bit is LOW, then a reception session is initiated and the UART0 continues to receive the following data bits (D0~D7). The bit value is decided by use of *majority decision*.
6. At the middle of the stop bit time, the UART0 checks the following conditions:
   a) RI0 must be LOW,
   b) if SM2 has been programmed to HIGH, then the received stop bit must also be HIGH. (If SM2 has been programmed to LOW, the received stop bit can be LOW or HIGH.)
7. If the above conditions are met, then the UART0 moves the received data byte from the temporary Receive Register (please refer to Fig.20) to SFR SBUF0, moves the received stop bit to the RB8 bit of SFR SCON0, and set RI0 bit to HIGH, triggering an UART0 data reception interrupt. If the above conditions are not met, the received data is ignored and the receive session is aborted.
8. After the middle of the stop bit time, the UART0 continues to wait for another high-to-low transition on the P3.0/RXD pin.

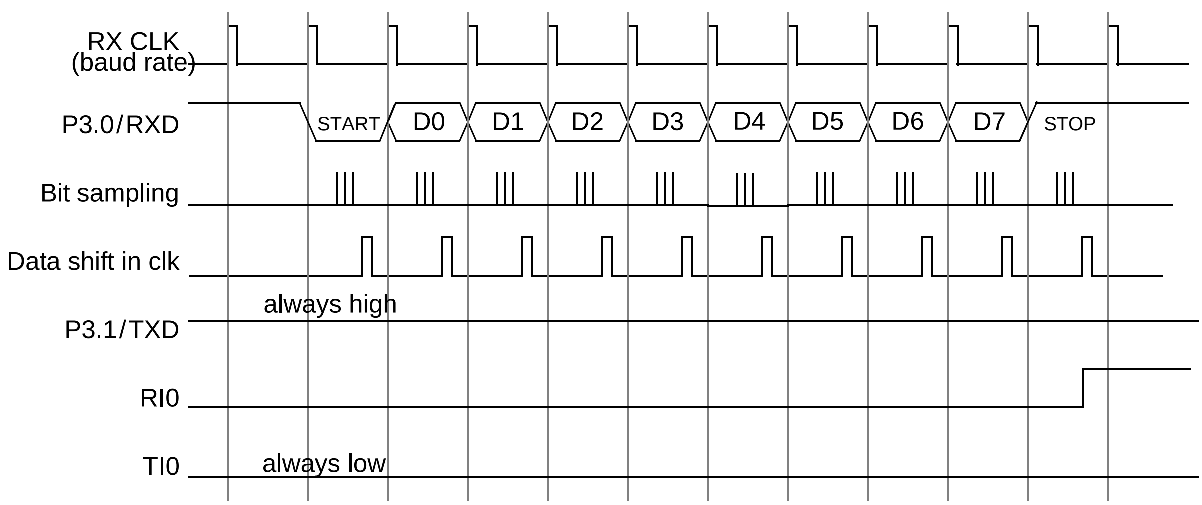


Fig.24 UART0 mode 1 reception timing

12.6 Mode 2

12.6.1 OPERATION OF MODE 2

Mode 2 provides 11-bits, asynchronous, full-duplex transmission or reception.

A transmission or reception word is composed of the following 11 bits:

- one start bit,
- eight data bits,
- one programmable 9th bit, and
- one stop bit.

The word format is shown below:

START	D0	D1	D2	D3	D4	D5	D6	D7	TB8/RB8	STOP

The data bits are transmitted and received LSB first.

For transmission, the 9th bit is determined by the value in TB8. To use the 9th bit as a parity bit, move the value of the P bit of SFR PSW to TB8.

12.6.2 BAUD RATE OF MODE 2

In Mode 2, the baud rate is decided by the value of the SMOD0 bit in the SFR PCON (please refer to Table 49).

- If SMOD0=0, the default value of SMOD0 after reset, the baud rate is $f_{xtal1}/64$. That is, the duration of a bit time is 64 XTAL1 clocks.
- If SMOD0=1, the baud rate is $f_{xtal1}/32$. That is, the duration of a bit time is 32 XTAL1 clocks.

12.6.3 DATA TRANSMISSION TIMING IN MODE 2

A data transmission session in mode 2 involves the following steps:

1. Application program issues a write to SFR SBUF0,
2. Transmission begins immediately after the first overflow of the divided-by-16 counter of the Baud Rate Generation circuit (please refer to Fig.27).
3. The UART0 transmits data out from the P3.1/TXD pin in the following order: START bit, data bits (D0~D7), and STOP bit. The START bit is transmitted out first.
4. The TI0 (SCON0.1) bit of SFR SCON0 is set to HIGH when the stop bit is placed on the P3.1/TXD pin.

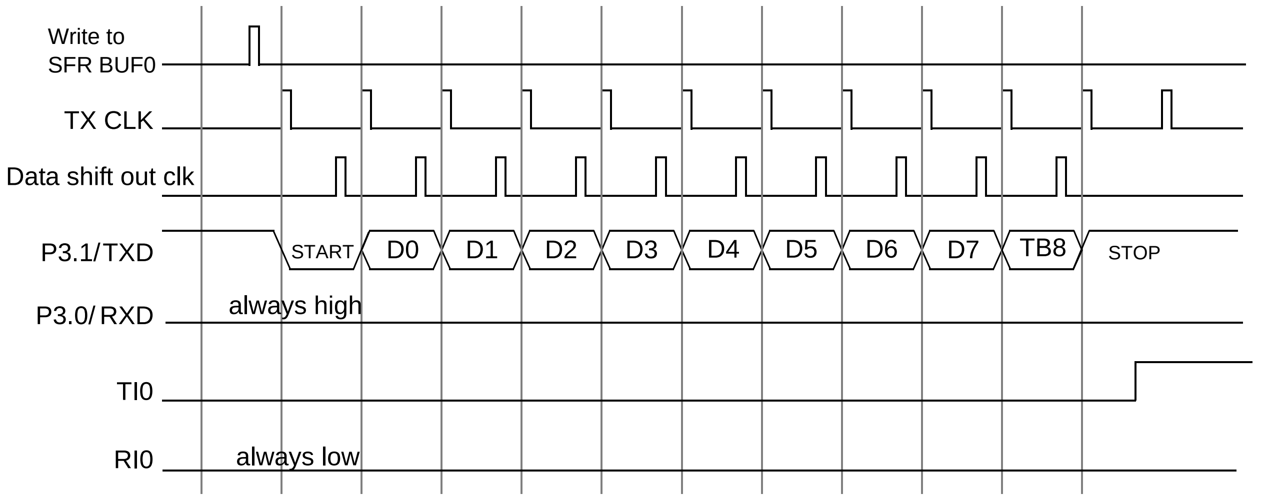


Fig.25 UART0 mode 2 transmission timing

12.6.4 Data reception timing in mode 2

A data reception session in mode 2 is as follows:

1. First, the reception function of the UART0 must be enabled by setting REN0=1 and then the UART0 starts detecting if there is a falling edge on the P3.0/RXD input. For detecting this falling edge, UART0 samples the P3.0/RXD input pin sixteen times per bit time for any baud rate.
2. When a falling edge on the P3.0/RXD pin is detected by UART0, the divided-by-16 counter of the baud rate generation circuit is reset. The output of the divided-by-16 counter is the receiver clock, RX CLK. This action is for aligning Timer 1 or Timer 2 overflow to bit boundaries. Please refer to Fig.27 for baud rate generation circuit.
3. For noise rejection, the UART0 decides the value of each received bit by *majority decision* of three consecutive samples in the middle of each bit time. That is, if three consecutive sampled values are 110, then the received bit value is regarded as HIGH. Similarly, if three consecutive sampled values are 101, then the received bit value is still regarded as HIGH.
4. If the first received bit is not LOW, then the reception session is aborted and the UART0 waits for another falling edge on the P3.0/RXD pin.
5. If the first received bit is LOW, then a reception session is initiated and the UART0 continues to receive the following data bits (D0~D7). The bit value is decided by use of *majority decision*.
6. At the middle of the stop bit time, the UART0 checks the following conditions:
   a) RI0 must be LOW,
   b) if SM2 has been programmed to HIGH, then the received 9th bit must also be HIGH. (If SM2 has been programmed to LOW, the received 9th bit can be LOW or HIGH.)
7. If the above conditions are met, then the UART0 moves the received data byte from the temporary Receive Register (please refer to Fig.20) to SFR SBUF0, moves the received 9th bit to the RB8 bit of SFR SCON0, and set RI0 bit to HIGH, triggering an UART0 data reception interrupt. If the above conditions are not met, the received data is ignored and the receive session is aborted.
8. After the middle of the stop bit time, the UART0 continues to wait for another high-to-low transition on the P3.0/RXD pin.

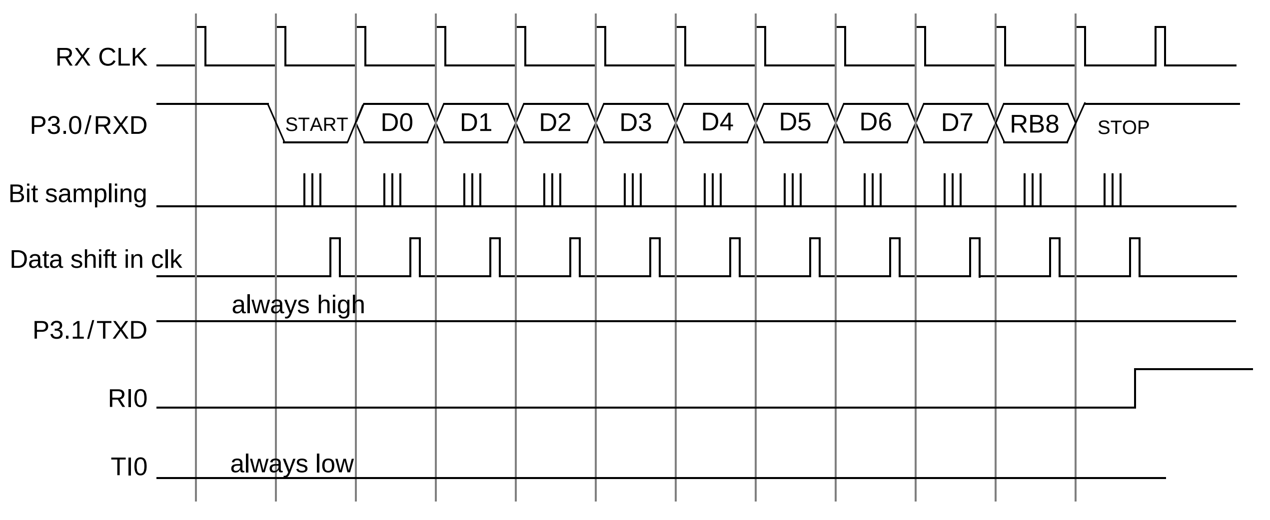


Fig.26 UART0 mode 2 reception timing

12.7 Mode 3

12.7.1 Operation of Mode 3

Mode 3 provides 11-bits, asynchronous, full-duplex transmission or reception. Its transmission or reception word format is composed of:

- one start bit,
- eight data bits,
- one programmable 9th bit, and
- one stop bit.

The word format is shown below. It is actually identical to that of Mode 2.

START	D0	D1	D2	D3	D4	D5	D6	D7	TB8/RB8	STOP

The data bits are transmitted and received LSB first.

Mode 3 operation is actually identical to Mode 2 operation, except baud rate. The Mode 3 baud rate generation is identical to Mode 1. That is, Mode 3 is a combination of Mode 2 transmission/reception protocol and Mode 1 baud rate generation.

12.7.2 Baud Rate of Mode 3

Mode 3 baud rate can be from timer 1 overflow or timer 2 overflow. Please refer to Section 12.8 “Baud Rate Generation for Mode 1 and Mode 3”

12.7.3 Data Transmission in Mode 3

Please refer to the description for mode 2.

12.7.4 Data Reception in Mode 3

Please refer to the description for mode 2.

12.8 Baud Rate Generation for Mode 1 and Mode 3

In both Mode 1 and Mode 3, baud rate is derived from **Timer 1** or **Timer 2** overflow. Fig.27 gives the divider circuit used to derive receiver baud rate and transmitter baud rate from Timer 1 overflow or Timer 2 overflow.

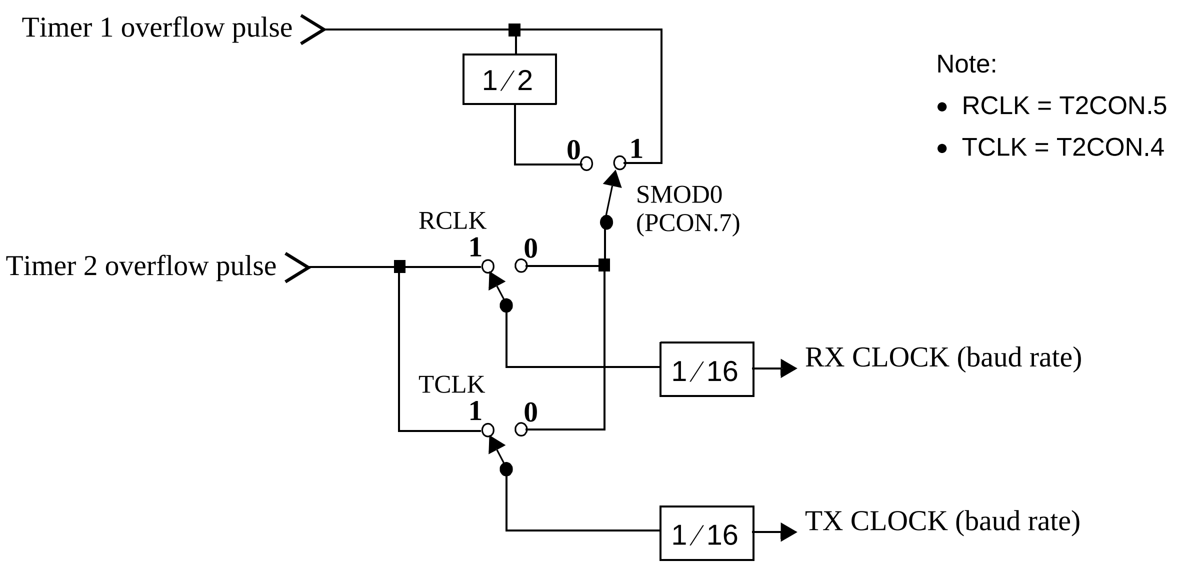


Fig.27 baud rate generation from Timer 1 or Timer 2 overflow

12.8.1 USING TIMER 1 TO GENERATE BAUD RATES

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD0 bit of the SFR PCON, as follows:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times \text{Timer1 overflow rate}$$

The Timer 1 interrupt should be disabled in this application.

The Timer 1 itself can be programmed for either **timer** or **counter** operation in any of its 3 running modes. In most typical applications, it is programmed for **timer** operation, in the Auto-Reload mode (high nibble of TMOD=0010B). In this case the baud rate is given by the formula:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times \text{XTAL1} \times \frac{1}{[12 \times (256 - \text{TH1})]}$$

By programming Timer 1 to run as a 16-bit timer (high nibble of TMOD=0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rate can be achieved

Table 36 lists sample reload values for a variety of common serial port baud rate.

Table 36 Timer 1 reload value for UART0 Mode 1 and Mode 3 baud rate.

Desired Baud rate	SMOD0 (PCON.7)	C/$\overline{T2}$ (TMOD.6)	Timer 1 Mode	33 MHz XTAL1	25 MHz XTAL1	11.0592 MHz XTAL1
57.6 Kb/s	1	0	2	FDh	FEh	FFh
19.2 Kb/s	1	0	2	F7h	F9h	FDh
9.6 Kb/s	1	0	2	EEh	F2h	FAh
4.8 Kb/s	1	0	2	DCh	E5h	F4h
2.4 Kb/s	1	0	2	B8h	CAh	E8h
1.2 Kb/s	1	0	2	71h	93h	D0h

12.8.2 USING TIMER 2 TO GENERATE BAUD RATES

Please refer to Section 11.6 “Baud Rate Generator Mode” for detailed description of using Timer 2 to generate baud rate for the UART0.

12.9 Multiprocessor communications

Mode 2 supports multiprocessor communication, in which a master transmitter can send data to one or more slave receivers. The 9th data bit is used to indicate an address byte or data byte. When the 9th data bit is HIGH, the transmitted byte is an address byte. When the 9th data bit is LOW, the transmitted byte is a data byte.

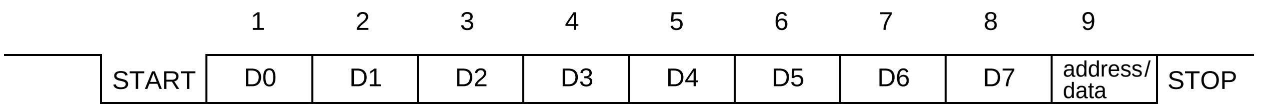


Fig.28 word format for multiprocessor communication

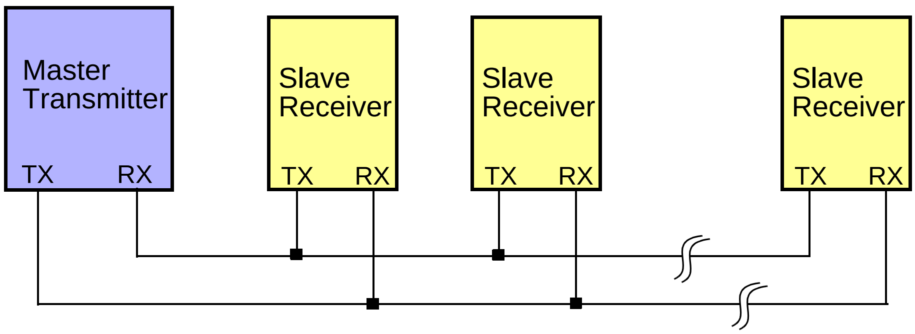


Fig.29 UART0 multiprocessor communication

A typical session of multiprocessor communication is as follows:

1. Enable all slave receivers for reception by setting REN=1 and clearing RI=0.
2. Setting SM2=1 for all slave receivers. SM=1 indicates that only an address byte, which has its 9th data bit set to HIGH, can be received by all slave receivers.
3. The master transmitter broadcasts an address byte out.
4. All the UART0s of all slave receivers receive this address byte and interrupt their respective CPU.
5. All slave receivers execute their UART0 interrupt subroutine.
6. In the interrupt subroutine, the received address is compared with the slave's pre-assigned address. If the two addresses match, then the SM2 bit is cleared to LOW. SM2=LOW indicates that the 9th bit data bit can be LOW or HIGH. That is, the addressed slave can always receive next transmitted data bytes from the master transmitter.
7. If the received address does not match with the slave's own pre-assigned address, the slave keeps its SM2 bit set to HIGH, indicating that the slave will not be able to received the next transmitted data bytes.
8. A communication channel is therefore established between the master transmitter and the addressed slave receiver. The master can continue to send data bytes to the addressed slave receiver. All other un-addressed slave receivers can not receive the following data bytes, because their SM2 bits remain at HIGH.
9. Once the entire message has been received, the addressed slave sets its SM2 bit to HIGH to block further interrupt and waits for the next address byte.

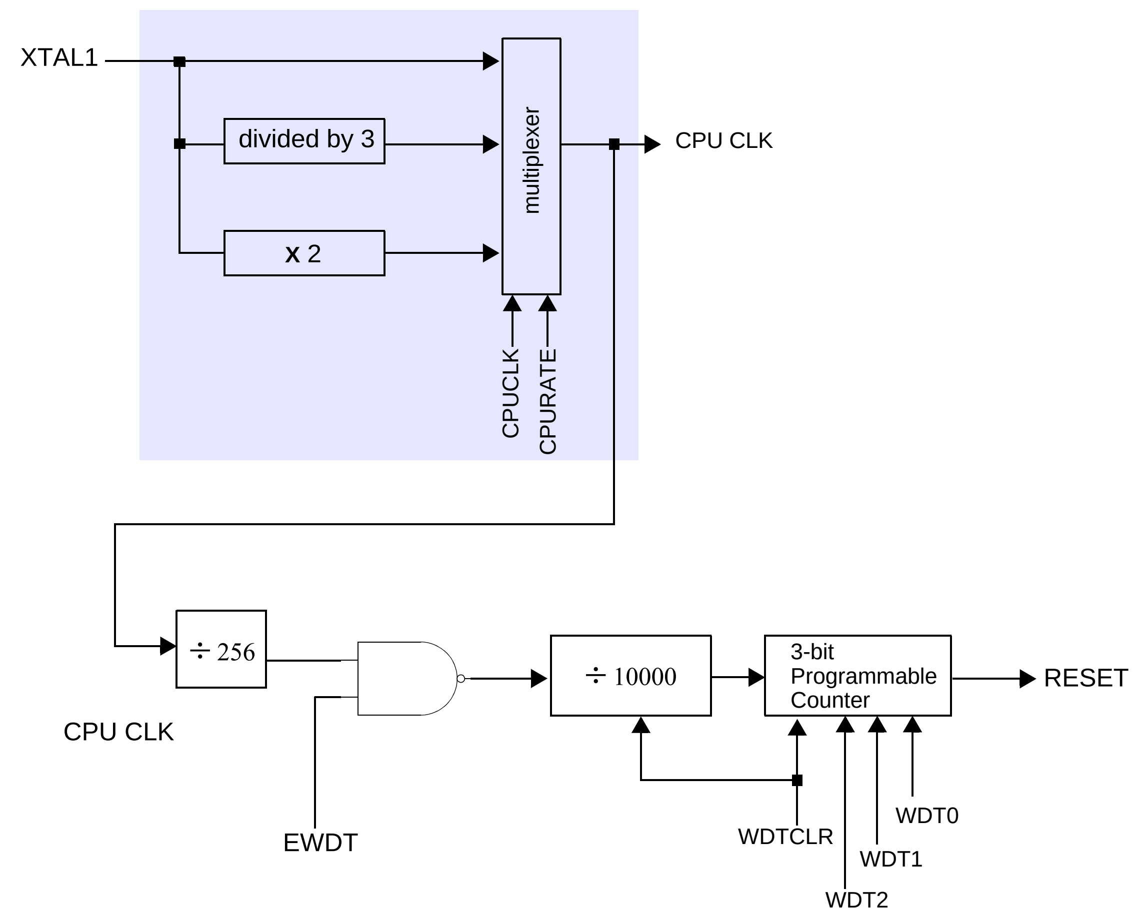
13 WATCHDOG TIMER

13.1 Functional Block Diagram

The Watchdog Timer is used to reset the STK6031 when it enters into an erroneous state, possibly due to disturbance from external world.

Only one SFR (SFR WDT), at SFR map address E1hex) is associated with the Watchdog Timer.

Fig.30 gives the functional block diagram of the Watchdog Timer.



Assuming that XTAL1= 24 MHz and CPU CLK is programmed to be equal to XTAL1, then the Watchdog Timer overflow period Δt can be calculated from the following equation:

$$\Delta t = N \times \frac{1}{24M} \times 256 \times 10000$$

Fig.30 Watchdog Timer.

13.2 Watchdog Timer Control Register

The Watchdog Timer Control Register (SFR WDT) is the only SFR associated with the Watchdog Timer. It can be written to or read from, and is described in Table 37.

Table 37 Watchdog Timer Register

WATCHDOG TIMER REGISTER, SFR WDT, AT E1 (HEX) OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	EWDT	WDTCLR	not implemented			WDT2	WDTI	WDT0
RESET value	0	0	x			0	0	0

Table 38 Description of SFR WDT

MNEMONIC	FUNCTION
EWDT (bit 7)	Enable Watchdog Timer. Setting EWDT=1 enables the Watchdog Timer. Setting EWDT=0 disables the Watchdog Timer.
WDTCLR (bit 6)	Setting WDTCLR= 1 clears the Watchdog Timer Programmable Counter and the divided-by-10000 prescaler. The Watchdog Timer must be regularly cleared before it overflows.
WDT2, WDT1, WDT0 (bits 2, 1, 0)	These 3 bits decides the overflow period of the Watchdog Timer. The following table gives the overflow period versus the values of these 3 bits, assuming that XTAL1=24 MHz and CPU CLK is programmed to be equal to XTAL1.

WDT2	WDT1	WDT0	Overflow interval	Notes
0	0	0	8 x 0.107 seconds	Assuming XTAL1=24 MHz and CPU CLK is programmed to be equal to XTAL1
0	0	1	1 x 0.107 seconds	
0	1	0	2 x 0.107 seconds	
0	1	1	3 x 0.107 seconds	
1	0	0	4 x 0.107 seconds	
1	0	1	5 x 0.107 seconds	
1	1	0	6 x 0.107 seconds	
1	1	1	7 x 0.107 seconds	

14 PWM (PULSE WIDTH MODULATED OUTPUT)

14.1 General description

The STK6031 contains 5 Pulse Width Modulated (PWM) outputs. These PWMs generate pulses of programmable length within an interval of 256 CPU clocks.

Six SFRs are associated with the PWM. They are listed in Table 39.

Table 39 SFRs for PWM

SYMBOL	DESCRIPTION	Address(Hex format)	RESET VALUE
P1_OTP	Port 1 pin selection for PWM output or Port 1 one pin output.	D1	xxx0 0000
PWM0D	PWM0 width	D2	1000 0000
PWM1D	PWM1 width	D3	1000 0000
PWM2D	PWM2 width	D4	1000 0000
PWM3D	PWM3 width	D5	1000 0000
PWM4D	PWM4 width	D6	1000 0000

When a PWM register (PWM0D ~ PWM4D) is loaded with a new value, the associated output is updated immediately. It does not have to wait until the end of the current counter period. All PWMn output pins are driven by push-pull output drivers.

Fig.31 gives functional diagram of the PWM.

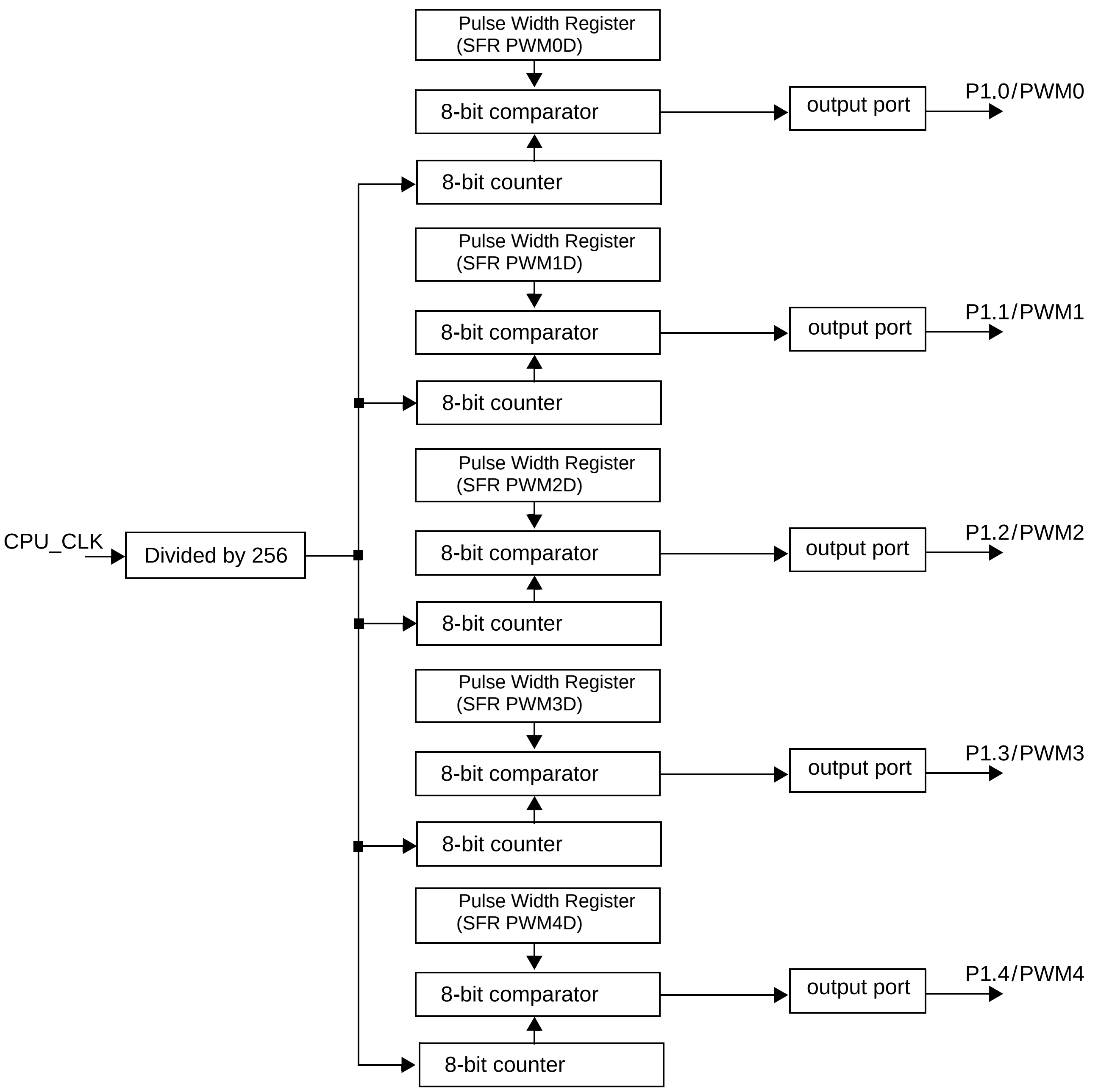


Fig.31 PWM functional block diagram

14.2 Port 1 Option Register (SFR P1_OPT)

The SFR P1_OPT is used to configure Port 1 pins to be Port 1 I/O pins or PWM output pins.

Table 40 Port 1 Option Register(address D1H)

Bit position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonics				PWM4E	PWM3E	PWM2E	PWM1E	PWM0E
Reset value	x	x	x	0	0	0	0	0

Table 41 Description of SFR P1_OPT bits

BIT	**SYMBOL**	**DESCRIPTION**
7, 6, 5	not implemented	
4 to 0	PWM4E to PWM0E	These bits are used to configure Port 4 pins to be an I/O pin or PWM output pin. When PWM4E=0, the P1.4/PWM4 pin works as an I/O pin. When PWM4E=1, P1.4/PWM4 pin works as PWM 4 output pin. Other bits can be configured in the same way.

14.3 Pulse Width Register 0 ~ 4 (PWM0D ~ PWM4D)

Table 42 Pulse width register (address D2 ~ D6 hex, R/W)

Register Name	**Address (hex)**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
PWM0D	D2	Pulse width of PWM channel 0.							
PWM1D	D3	Pulse width of PWM channel 1.							
PWM2D	D4	Pulse width of PWM channel 2.							
PWM3D	D5	Pulse width of PWM channel 3.							
PWM4D	D6	Pulse width of PWM channel 4.							
Reset value		1	0	0	0	0	0	0	0

The value of a Pulse Width Register indicates the HIGH pulse width within an interval of 256 CPU clocks, as illustrated in Fig.32.

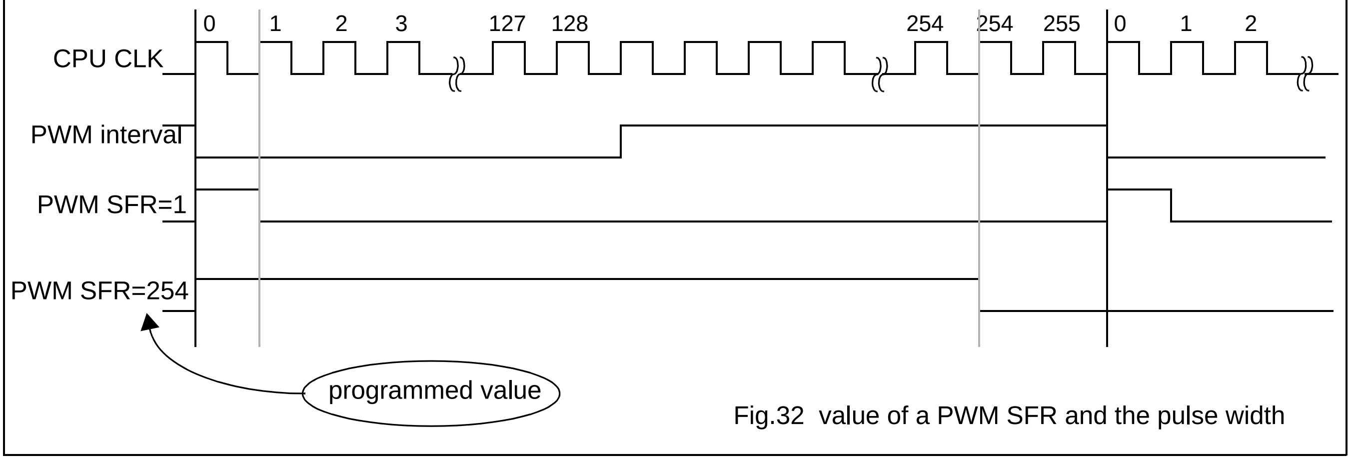


Fig.32 value of a PWM SFR and the pulse width

15 ANALOG-TO-DIGITAL CONVERTER (ADC)

15.1 ADC functional description

The STK6031 has a 6-bit successive approximation ADC with 4 multiplexed analog input channels. ADC channel inputs share with Port 4 pins. Analog input voltage range can be from 0 V to 3.3 V.

Three SFRs (P4_OPT, ADCSEL, and ADCVAL) perform the user software interface to the ADC; see Table 43 for an overview of the ADC SFRs.

Figure 33 shows the relation between SFRs and the ADC.

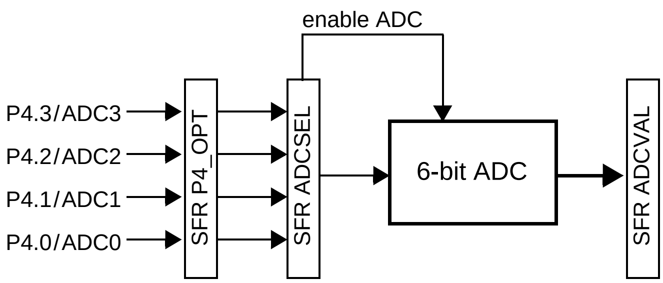


Fig.33 ADC SFRs

15.2 ADC during Idle and Stop mode

The analog-to-digital converter is active only when the microcontroller is in normal operating mode. If the Idle or Stop mode is activated, then the ADC is switched off and put into a power saving idle state - a conversion in progress is aborted. The conversion result register (SFR ADCVAL) is not affected.

15.3 ADC SFRs and their reset value

Three SFRs (P4_OPT, ADCSEL, and ADCVAL) are associated with ADC. An overview of these three registers is given in Table 43.

Table 43 ADC Special Function Registers overview

ADDRESS	NAME	R/W	DESCRIPTION
D9(hex)	P4_OPT	R/W	Selection of Port 4 pin function.
DA(hex)	ADCSEL	R/W	Channel selection.
DB(hex)	ADCVAL	R/W	ADC value.

15.3.1 P4_OPT Register

The P4_OPT SFR has only 4 bits. It is used to configure Port 4 pins either as a port pin or as an analog input pin for the 6-bit ADC.

Table 44 P4_OPT register (address D9 hex)

Bit Number	BIT 7	BIT 6	BIT 5	4 BIT	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	not physically implemented				ADC3E	ADC2E	ADC1E	ADC0E
Rest Value	x	x	x	x	0	0	0	0

Table 45 Description of P4_OPT Register bits

BIT	SYMBOL	DESCRIPTION
3	ADC3E	ADC3E=1 configures pin P4.3/ADC3 as an analog input pin. ADC3E=0 configures pin P4.3/ADC3 as a port pin (P4.3)
2	ADC2E	ADC2E=1 configures pin P4.2/ADC2 as an analog input pin. ADC2E=0 configures pin P4.2/ADC2 as a port pin (P4.2)
1	ADC1E	ADC1E=1 configures pin P4.1/ADC1 as an analog input pin. ADC1E=0 configures pin P4.1/ADC1 as a port pin (P4.1)
0	ADC0E	ADC0E=1 configures pin P4.0/ADC0 as an analog input pin. ADC0E=0 configures pin P4.0/ADC0 as a port pin (P4.0)

15.3.2 THE ADCSEL REGISTER

The ADCSEL Register is used to select an input channel for conversion. For proper conversion of the input analog voltage, do the following:

1. Select a channel for analog signal input,
2. Then, enable the ADC by setting the EADC bit to HIGH.

Table 46 ADCSEL Register (address DA hex)

Bit Number	**BIT 7**	**BIT 6**	**BIT 5**	**4 BIT**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Bit Name	EADC	not physically implemented			SAD3	SAD2	SAD1	SAD0
Reset Value	0	x	x	x	0	0	0	0

Table 47 Description of ADC Register bits

BIT	SYMBOL	DESCRIPTION
7	EADC	Enable the ADC.
3	SADC3	SADC3=1 selects analog signal from P4.3/ADC3 pin for conversion. SADC3=0 un-selects this pin.
2	SADC2	SADC2=1 selects analog signal from P4.2/ADC2 pin for conversion. SADC2=0 un-selects this pin for conversion.
1	SADC1	SADC1=1 selects analog signal from P4.1/ADC1 pin for conversion. SADC1=0 un-selects this pin for conversion.
0	SADC0	SADC0=1 selects analog signal from P4.0/ADC0 pin for conversion. SADC0=0 un-selects this pin for conversion.

15.3.3 ADCVAL REGISTERS

The binary result code of the analog-to-digital conversions is stored in the ADCVAL Register.

Table 48 ADCVAL Register (address DB hex)

Bit Number	**BIT 7**	**BIT 6**	**BIT 5**	**4 BIT**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Bit Name	x	x	Binary code of the ADC conversion.					
Reset Value	x	x	0	0	0	0	0	0

15.4 ADC resolution and characteristics

The analog input voltage should be stable when the ADC is enabled to perform conversion. An RC low pass filter may be added to the analog input pins to filter out high frequency noises.The capacitor between an analog input pin and the ground pin shall be placed as close to the pins as possible, in order to have maximum effect in minimizing input noise coupling.

Fig.34 gives the converted digital value (given in decimal unit) versus input analog voltages.

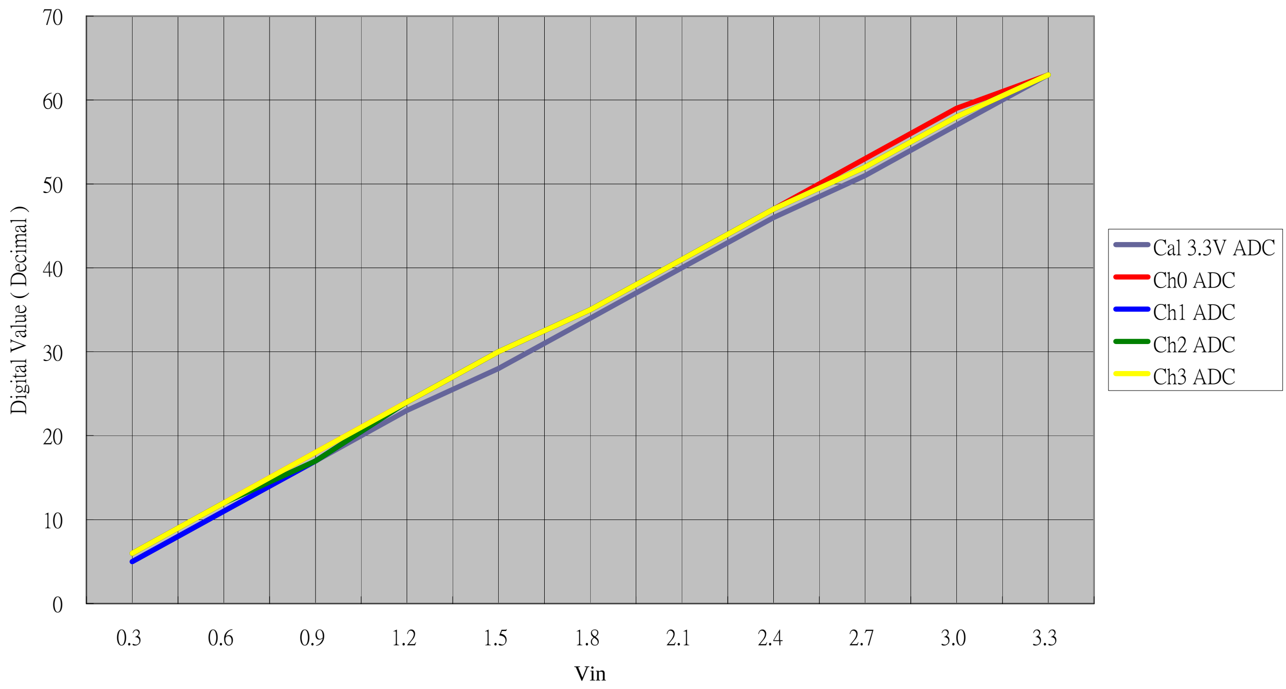


Fig.34 Converted digital code versus analog input voltage.

16 OSCILLATOR CIRCUIT

16.1 The Oscillator Circuit

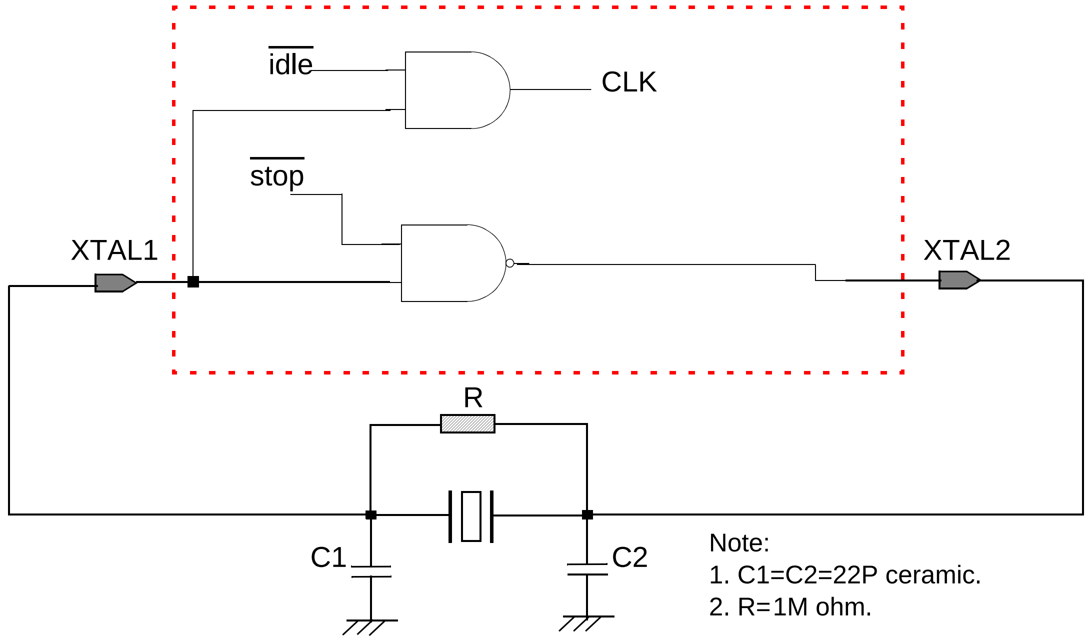


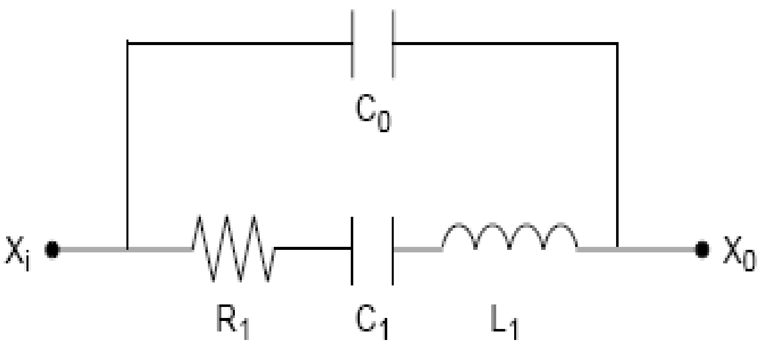
Fig.35 Oscillator Circuit.

XTAL1 is the high gain amplifier input, and XTAL2 is the output. To drive the STK6031 externally, XTAL1 is driven from an external clock source and XTAL2 is left open.

16.2 The values for R, C1, and C2

The recommended values for R, C1, and C2 given Fig.35 is for the frequency range from 2M Hz to 30M Hz.

Since the performance of the crystal oscillator is closely related to the characteristics of the crystal itself, the user should contact the crystal manufacturer for its characteristics. The crystal parameters we used for design is shown in Fig.36.



The parameter for the crystal is:
R1=10 ohm, C1=25 fF, and
C_0=7 pF.

Fig.36 crystal parameters

17 RESET

17.1 Sources of RESET

There are 5 sources to reset STK6031:

- external RESET pin,
- power-on reset,
- low-voltage detection reset,
- watchdog timer overflow, and
- ISP programming.

The functional diagram of the reset circuit is shown in Fig.37.

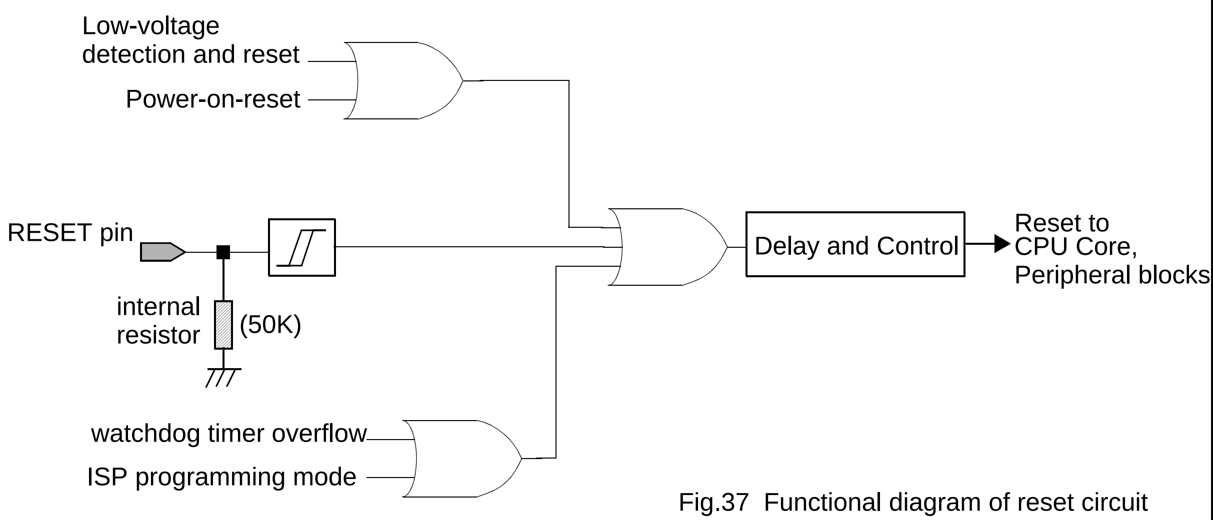


Fig.37 Functional diagram of reset circuit

17.2 Power-On- Reset (POR) with fast-rising power supply

The STK6031 can be reset by the on-chip power-on-reset, whose switching level is 2.7 ± 0.2 volts. The sequence of the power-on-reset is as follows:

1. As soon as the power supply (VDD) reaches the POR switching level, the on-chip POR generates a pulse, called POR Pulse.
2. This POR pulse then triggers an internal reset, POC. Also, this POR pulse resets the internal reset counter.
3. When the oscillator is stable enough, the oscillator clocks starts triggering the internal reset counter to count.
4. When the internal reset counter counts up to 2048 and overflows, the internal reset (POC) is released and the CPU starts executing instruction.

The above sequence is further illustrated in Fig.38.

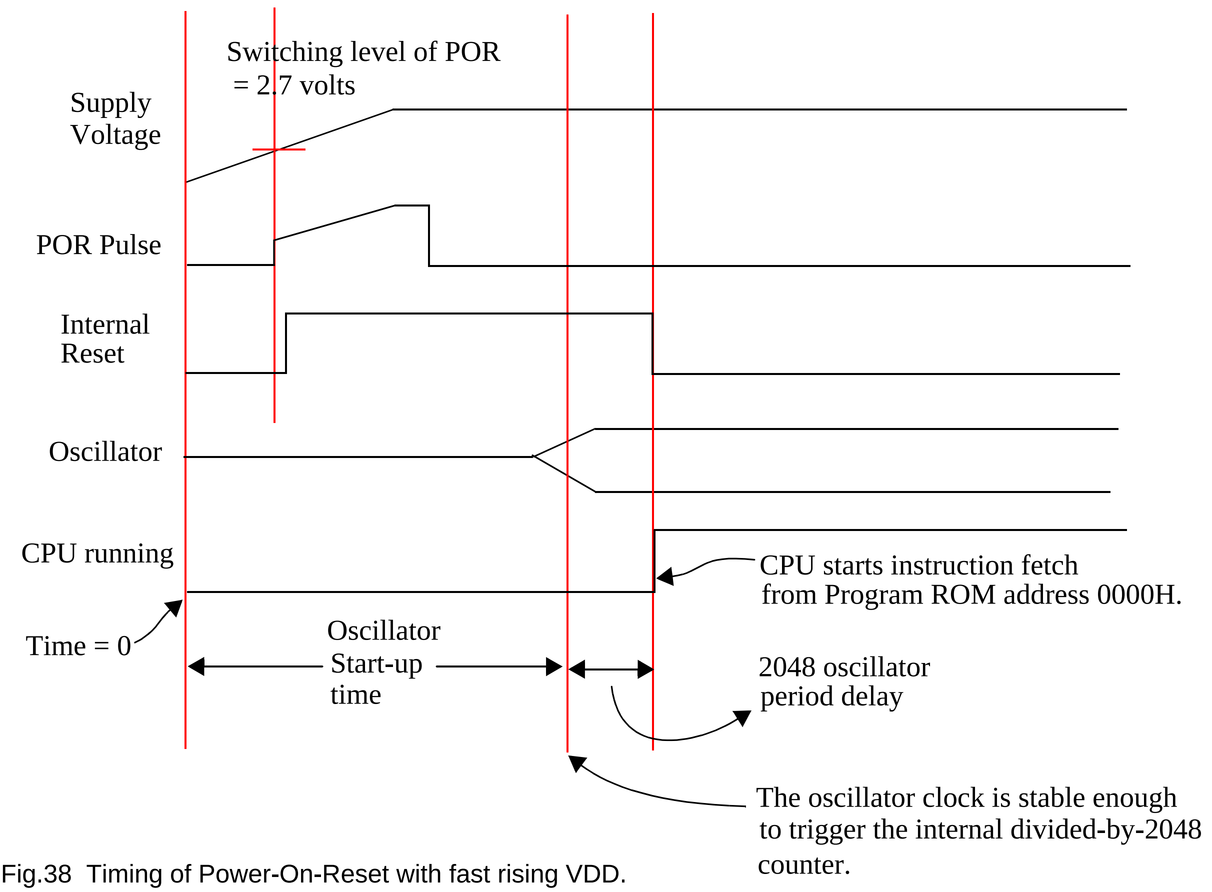


Fig.38 Timing of Power-On-Reset with fast rising VDD.

17.3 Asynchronous reset by adding a HIGH pulse to the RESET pin

The STK6031 can be reset by adding a HIGH pulse to the RESET pin. The RESET pin is an input with an internal Schmitt-trigger for noise reduction. The CPU checks if there is a reset at cycle 4 (C4) of every instruction cycle. A reset is accomplished by holding the RESET pin HIGH for at least two instruction cycles while the oscillator is running. The CPU responds by executing an internal reset.

17.4 Low-power detection and reset

The STK6031 has the capability of low-power detection and reset. The reset due to low power can be enabled or disabled by use of the LVR bit (bit 0) of SFR CHIPCON, at SFR address BF(hex). Setting LVR=0 enables low-power reset and setting LVR=1 disables low-power reset.

Due to fabrication process variations from different production lots, the threshold voltage for low-power detection is in the range of 2.52 ~ 2.94 volts, without regard to the supply voltage to the VDD pin. The typical low-power threshold voltage is 2.7 volts.

17.5 Reset by the Watchdog Timer overflow

The microcontroller can also be reset by the Watchdog Timer overflow. Please refer to Chapter 13 .

18 POWER-SAVING MODES

The STK6031 provides two power-saving modes: **Idle mode** and **Stop mode**. The bits that control entry into Idle mode and Stop modes are bits 0 (Idle mode) and bit 1 (Stop mode) of the Power Control Register (SFR PCON) at SFR address 87(hex). Table 49 gives a description of the Power Control Register (SFR PCON).

Table 49 Power Control Register (SFR PCON)

Bit	Mnemonics	Function
PCON.7	SMOD0	UART baud-rate doubler enable. When SMOD0=1, the baud rate for the UART is doubled. Please refer to Fig.19.
PCON. 6~4		Reserved.
PCON.3	GF1	General purpose flag 1. Bit-addressable, general-purpose flag for software control.
PCON.2	GF0	General purpose flag 0. Bit-addressable, general-purpose flag for software control.
PCON.1	STOP	STOP mode select. Setting the STOP=1 places the STK6031 in STOP mode.
PCON.0	IDLE	IDLE mode select. Setting the IDLE=1 places the STK6031 in IDLE mode.

If the STOP Mode and the Idle Mode are selected at the same time, the STOP Mode has higher priority, as can be obviously seen in Fig.39

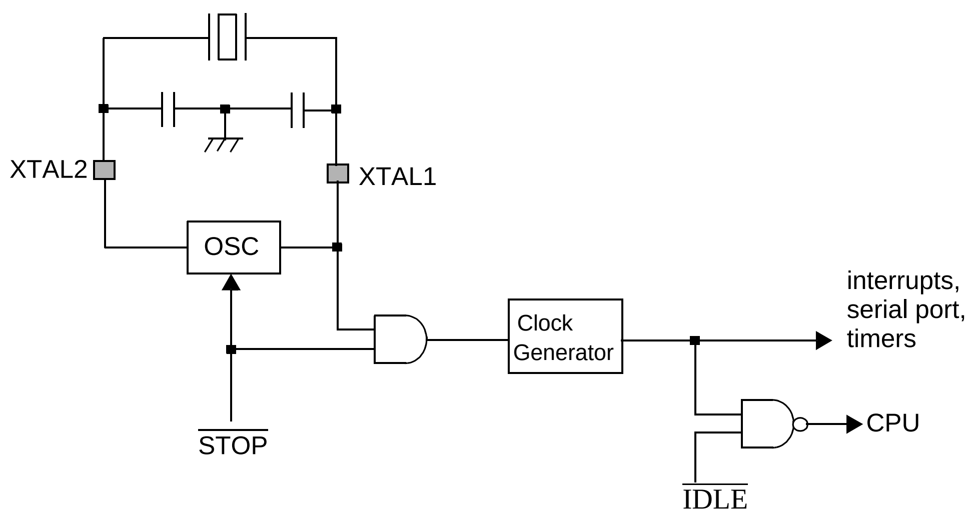


Fig.39 Power-saving modes.

18.1 Idle Mode

Idle mode operation permits the interrupt, serial ports and timers to function while the CPU is halted. The functions that are switched off when the microcontroller enters the Idle mode are:

- CPU (halted)

The functions that remain active during Idle mode are:

- Timer 0, Timer 1, Timer 2, and Watchdog Timer
- UART
- External/Internal interrupts
- External reset or power-on-reset.

The instruction that sets PCON.0 (=1) is the last instruction executed in the normal operating mode before Idle mode is activated.

Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their current data during Idle mode. The status of external pins during Idle mode is shown in Table 50.

There are three ways to terminate the Idle mode:

- Activation of any enabled interrupt from interrupt sources listed in Table 12 will cause PCON.0 to be cleared by hardware, terminating Idle mode, but only if there is no interrupt in service with the same or higher priority. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

  The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during Idle mode.

  For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits.

  When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
- The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two instruction cycles to complete the reset operation.
- The third way of terminating the Idle mode is by internal watchdog reset.

18.2 Stop mode

The instruction that sets PCON.1 is the last executed, prior to going into the Stop mode. Once in Stop mode, the crystal oscillator is stopped. The contents of the on-chip RAM (AUX Memory and Main Data Memory) and the SFRs are preserved.

Note that the Stop mode can not be entered when the Watchdog Timer has been enabled.

The Stop mode can be terminated only by an external reset (RAM is saved, but SFRs are cleared due to reset).

The status of the external pins during Stop mode is shown in Table 50.

In the Stop mode, Vdd supplies to the CPU can be reduced to minimize power consumption. It must be ensured, however, that Vdd is not reduced before the Stop mode is activated, and that the Vdd is restored to its normal operating level before the Stop mode is terminated by hardware reset. The reset signal that terminates the Stop mode also restarts the oscillator.The reset signal should not be activated before Vdd is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize(similar to power-on reset).

18.3 Status of external pins during power-saving modes

Table 50 Status of external pins during Idle and Stop modes.

MODE	Memory	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
Idle	internal	1	1	port data	port data	port data	port data	port data
	external	1	1	high-Z	port data	address	port data	port data
Stop	internal	0	0	port data	port data	port data	port data	port data
	external	0	0	high-Z	port data	port data	port data	port data

18.4 Summary of Power-saving Modes

Table 51 .Summary of power-saving modes

MODE	Example for enabling the mode	TERMINATED BY	REMARKS
Idle	ORL PCON, #01H	• Enabled interrupt • External hardware reset • Watchdog Timer overflow.	• CPU is gated off • CPU status registers maintain their data. • Peripherals are active.
Stop	ORL PCON, #02H	External hardware reset	• Crystal oscillator is stopped. • Contents of on-chip RAM and SFRs are maintained. • However, leaving Power- Down mode means redefinition of SFR contents.

19 PORT 0, PORT 1, PORT 2, PORT 3, AND PORT 4

19.1 General Description

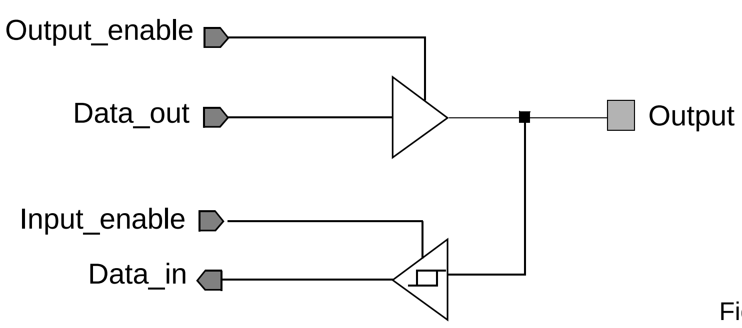
The STK6031 has four 8-bits ports (Ports 0 ~ 3)and one 4-bit port (Port 4). All bits of Port 0 are push-pull output. All bits of Port 1, Port 2, Port 3 and Port 4 are push-pull outputs with internal weak pull-high PMOS.

19.2 Port 0

Port 0 pins are push-pull outputs. It has three functions:

- Pure bidirectional I/O data ports
- Low-byte address (A0 ~ A7) output and OP code input, when executing program in external program ROM mode ($\overline{EA}$= 0, during power-on reset).
- Low-byte address (A0 ~ A7) and data bus during read/write to off-chip AUX memory.

SFR P0_OPT must be properly programmed to ensure proper operation of Port 0.



Port 0 pins are push-pull outputs. The output sinking and sourcing capability is 4 mA (typ.).

Fig.40 Port 0 schematics

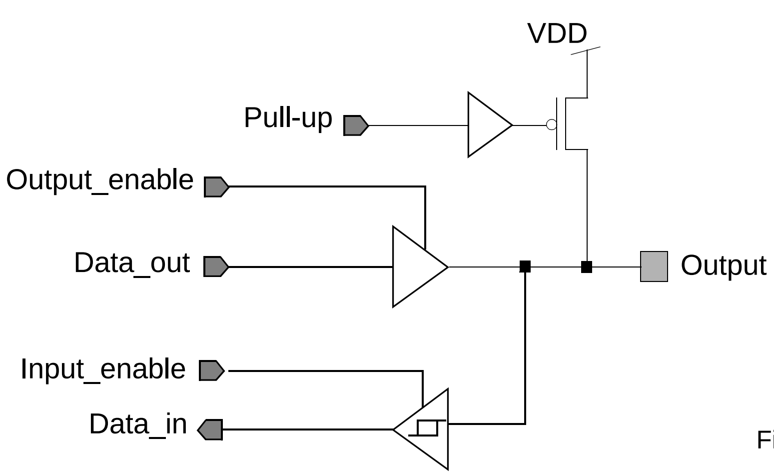
19.3 Port 1, Port 2, and Port 3

Figure 41 shows Port 1, Port 2, and Port 3. They are push-pull outputs with internal weak pull-up.

Port 1shares with the 5-channel, 8-bit, PWM for data input/output. SFR P1_OPT needs to be properly programmed to ensure proper operation of Port 1. Please refer to Section 14.2 for detailed description of SFR P1_OPT.

Port 2 acts as data I/O or address bus (A8 ~ A15) during access to external Program ROM and AUX memory. SFR P2_OPT must be properly programmed to ensure proper operation of Port 2.

Port 3 are multi-functional I/O port.

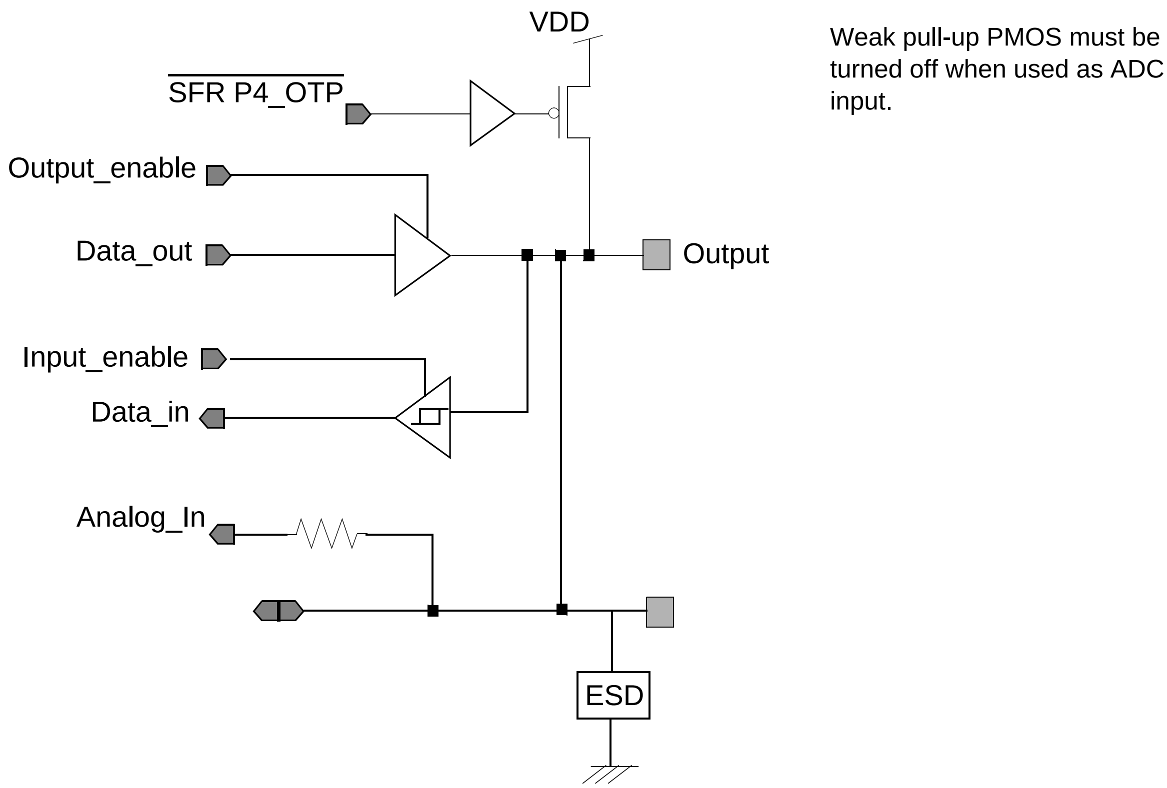


Pins of Port 1, Port 2, and Port 3 are push-pull outputs with weak internal pull-up. The output sinking and sourcing capability is 4 mA (typ.). The typical value of the equivalent resistance of the pull-up PMOS is 15K ohm.

Fig.41 Port 1, Port 2, and Port 3

19.4 Port 4

Port 4 share inputs with the 6-bit ADC. SFR P4_OPT needs to be properly programmed to ensure the proper operation of Port 4. Please refer to Section 14.2 for detailed description of Port 4.



19.5 MOVX instruction, Port 0, Port 2, P3.6, P3.7

When executing MOVX instruction from internal program memory, an access to the internal AUX RAM will not affect Port 0, Port 2, P3.6 and P3.7.

19.6 Multiple-Function Port Pins

Some port pins have multiple functions. Port pins which are not used for alternate functions may be used as normal bidirectional I/O pins. The configuration of a port pin as an alternate function is carried out automatically by writing the associated SFR bit with proper value.

Please refer to Table 2 for a detailed description of multiple-function pins.

20 ABSOLUTE MAXIMUM RATING

Table 52 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
VDD	voltage on VDD with respect to ground, and SCL, SDA to ground.	–0.3	+3.8	volts
V_I (note 1)	input voltage on any other pin with respect to ground, except 5V-tolerant I/Os.	–0.3	VDD + 0.3	volts
I_I, I_O	input/output current on any I/O pin		±15	mA
I_{total}	Absolute sum of all input currents during overload condition.		100	mA
P_{tot}	total power dissipation (note 2)		1.5	W
T_{stg}	storage temperature range.	–40	+125	°C
T_{amb}	operating ambient temperature range.	-20	+ 85	°C

Notes

1. The following applies to the Absolute Maximum Ratings:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device should refer to the normal DC and AC characteristics.
   b) This product includes ESD-protection circuits, specifically designed for the protection of its internal circuit. However, its suggested that conventional ESD precautions be taken.
   c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to ground.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package, not on device power consumption.

21 DC/AC CHARACTERISTICS

Table 53 DC/AC characteristics

Test condition: V_{DD} = 3.3 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} , unless otherwise specified; T_{amb} = -20 to +85 °C; f_{XTAL1} = 24 MHz

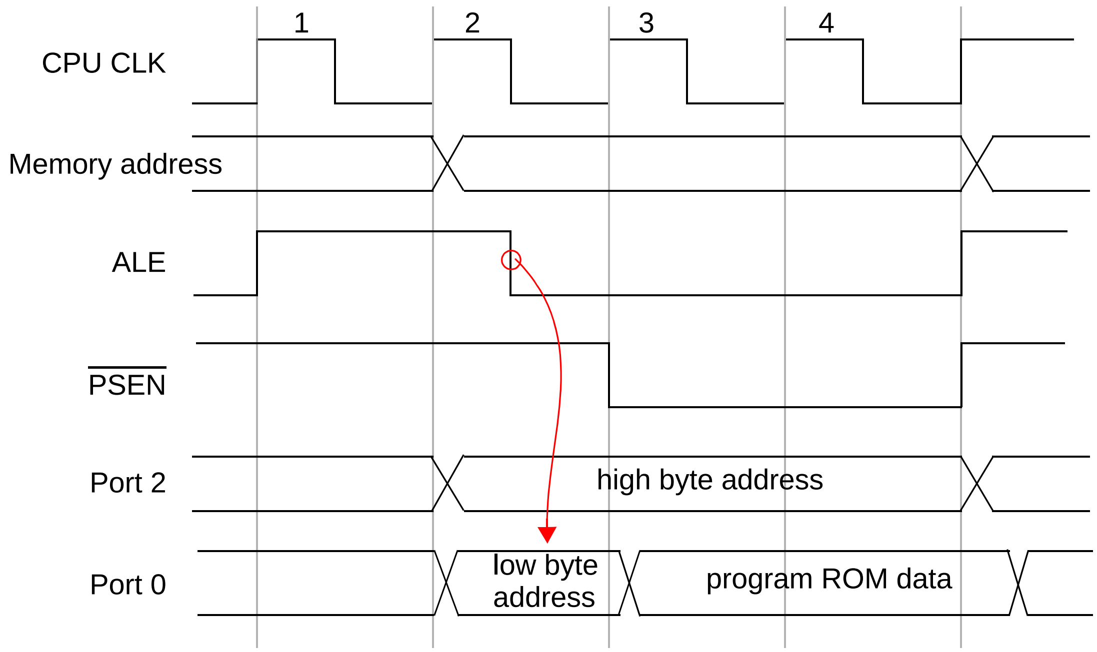
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
VDD	Operating supply voltage.		2.7		3.6	V
$T_{operating}$	Operating temperature range		-20		85	°C
$F_{operating}$	Operating frequency range		2 MHz	24 MHz	30 MHz	
$I_{DD(NORMAL)}$	operating supply current in normal mode.	notes 1, 2 and 3		8		mA
$I_{DD(IDLE)}$	supply current in Idle mode	notes 1 ,2 and 3		3.5		mA
$I_{DD(STOP)}$	supply current in Stop mode	notes 1 ,2 and 3		10		µA
Current sourcing/sinking capability of Ports 0, 1, 2, 3, 4, at VDD=3.0 volts						
I_{P0_sink}	The open-drain NMOS sinking current of Port 0.			4		mA
I_{P1_source}	The PMOS sourcing current of Port 1.			200		µA
I_{P1_sink}	The NMOS sinking current of Port 1.			4		mA
I_{P2_source}	The PMOS sourcing current of Port 2.			200		µA
I_{P2_sink}	The NMOS sinking current of Port 2.			4		mA
I_{P3_source}	The PMOS sourcing current of Port 3.			200		µA
I_{P3_sink}	The NMOS sinking current of Port 3.			4		mA
I_{P4_source}	The PMOS sourcing current of Port 4.			200		µA
I_{P4_sink}	The NMOS sinking current of Port 4.			4		mA
Current sourcing/sinking capability of the ALE pin and the $\overline{PSEN}$ pin, at VDD=3.0 volts						
I_{ALE_source}	The PMOS sourcing current of the ALE pin.			4		mA
I_{ALE_sink}	The NMOS sinking current of the ALE pin.			4		mA
$I_{\overline{PSEN}\_source}$	The PMOS sourcing current of the $\overline{PSEN}$ pin.			4		mA
$I_{\overline{PSEN}\_sink}$	The NMOS sinking current of the $\overline{PSEN}$ pin.			4		mA
Inputs HIGH/LOW voltage, Output HIGH/LOW voltage at VDD=3.0 volts.						
V_{OL_P0}	Output LOW voltage of Port 0.	I_{OL} = 3.2 mA; note 5	0.0	0.144	0.4	volts

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input LOW voltage to Port 0, Port 1, Port 2, Port 3, and Port 4.		-0.5		0.8	volts
V_{IH}	Input HIGH voltage to Port 0, Port 1, Port 2, Port 3, and Port 4.		2.3		5.5 (5V-tolerant)	volts
V_{OL}	Output LOW voltage of Port 1, Port 2, Port 3, and Port 4.	I_{OL} = 3.2 mA; note 5	0.0	0.139	0.4	volts
V_{OH}	Output HIGH voltage of Port 0, Port 1, Port 2, Port 3 and Port 4.	I_{OH} = -25 μA	2.4	2.895	3.6	volts
V_{IH_RST}	Input HIGH voltage to RESET pin.		2.54			volts
V_{IL_RST}	Input LOW voltage to RESET pin.				0.8	volts
V_{OL_ALE}	Output LOW voltage of ALE pin.	I_{OL} = 3.2 mA; note 5	0.0		0.4	volts
V_{OH_ALE}	Output HIGH voltage of ALE pin.	I_{OH} = -60 μA	2.4		3.6	volts
$V_{OL\_\overline{PSEN}}$	Output LOW voltage of $\overline{PSEN}$ pin.	I_{OL} = 3.2 mA; note 5	0.0		0.4	volts
$V_{OH\_\overline{PSEN}}$	Output HIGH voltage of $\overline{PSEN}$ pin.	I_{OH} = -60 μA	2.4		3.6	volts
$C_{I/O}$	I/O pin capacitance	test frequency = 1 MHz; T_{amb} = 25 °C	–		10	pF

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 5ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ - 0.5 V; Port 0 = V_{DD}; $\overline{EA} = V_{SS}$.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 5ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ - 0.5 V; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}.
3. The Stop current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = V_{DD}; $\overline{EA}$ = XTAL1 = V_{SS}.
4. Pins of Ports 1, 2, 3, and 4 source a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when V_{IN} is approximately 1.6 V.
5. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
6. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} ; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ - 0.5 V; XTAL2 not connected; Port 0 = V_{DD}; $\overline{EA}$ = XTAL1 = V_{SS}.

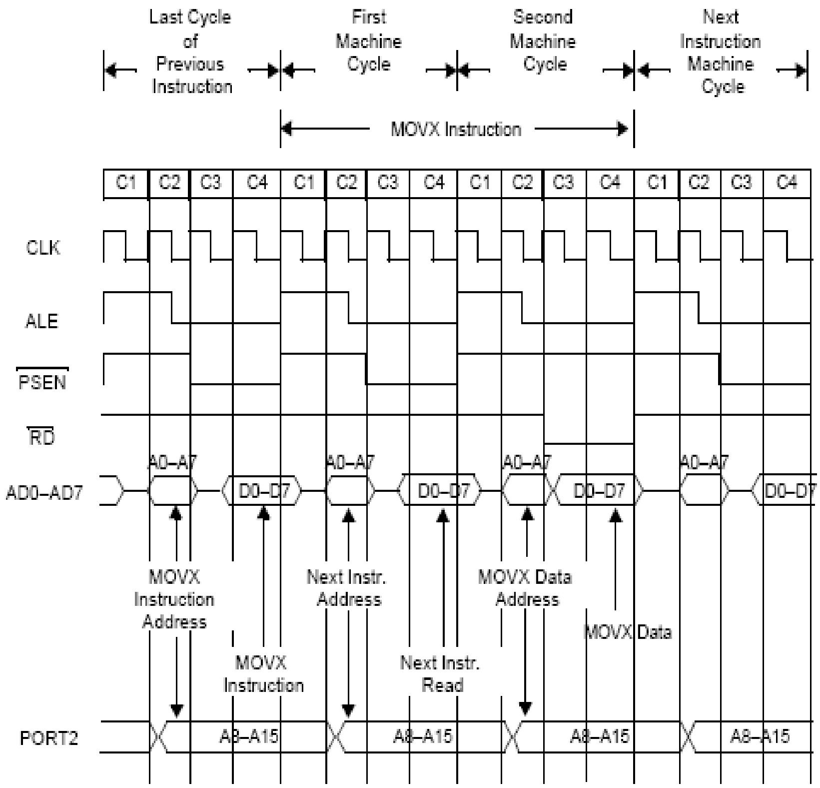
22 EXTERNAL PROGRAM MEMORY READ CYCLE

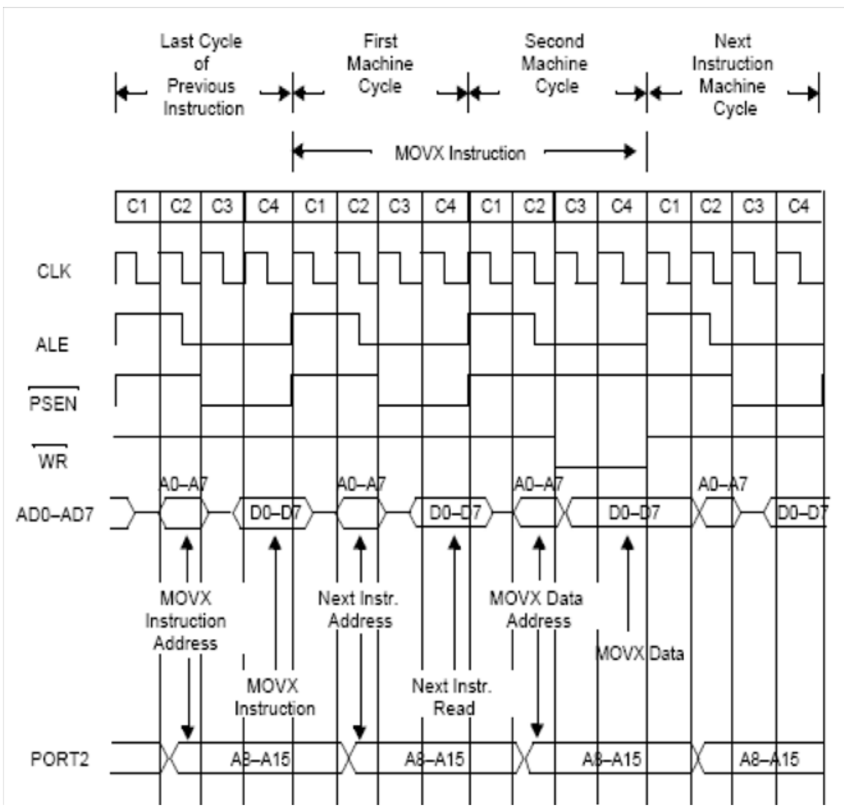


Note:
For external program ROM read, the $\overline{EA}$ input pin must be connected to LOW before Power-On-Reset.

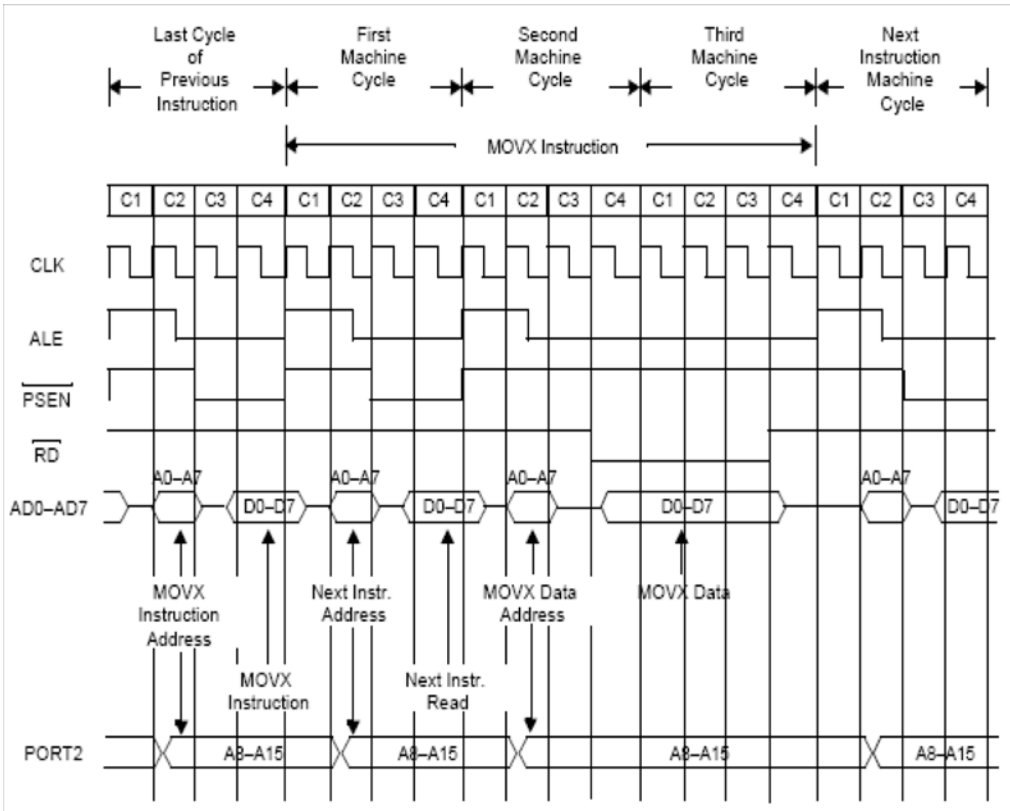
Fig.42 External program memory read cycle

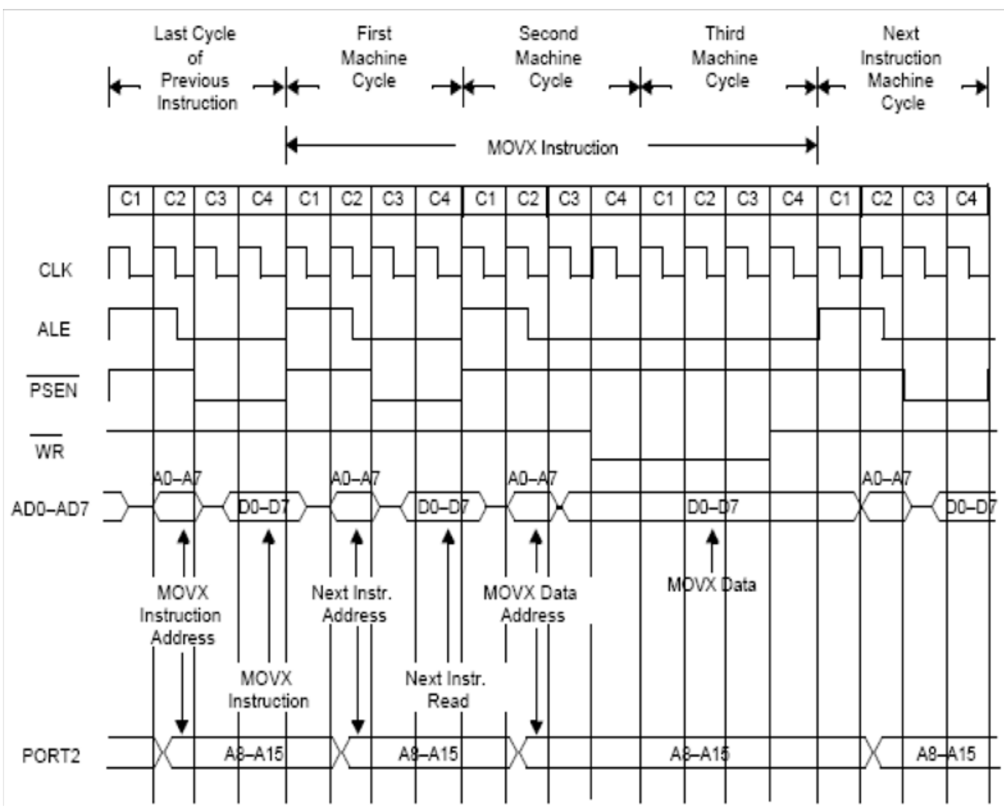
23 EXTERNAL AUX MEMORY READ/WRITE TIMING WITH STRETCH= 0



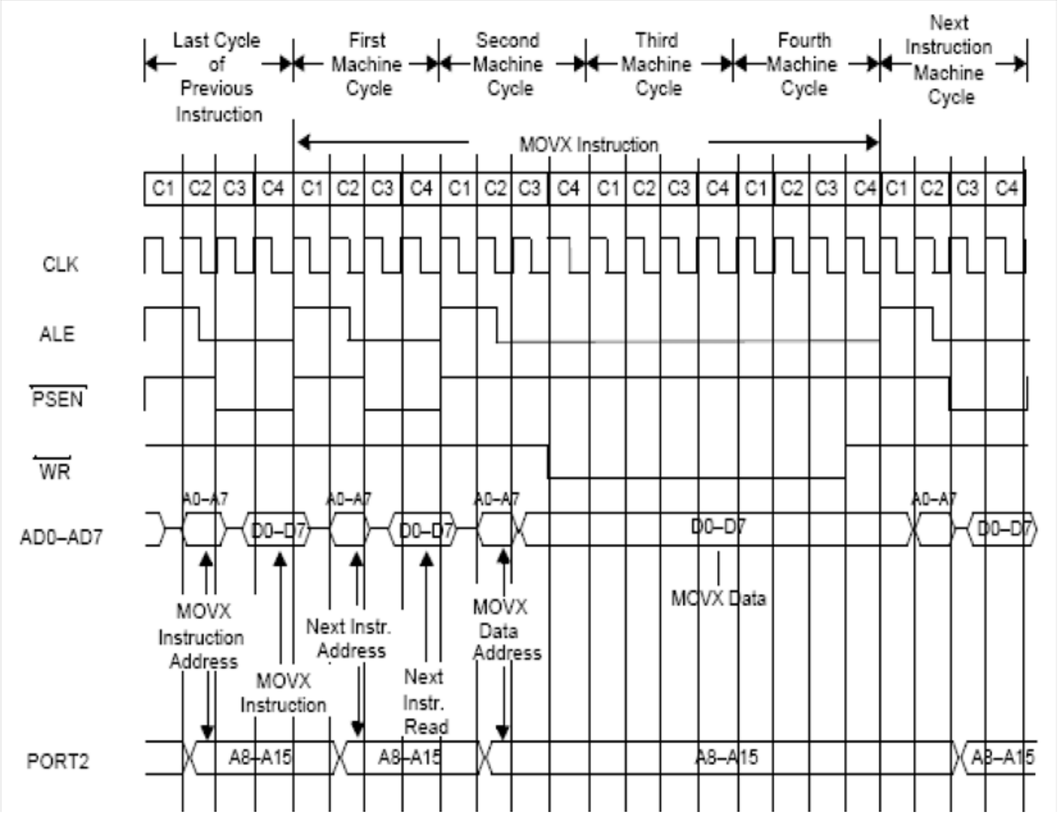


24 EXTERNAL AUX MEMORY READ/WRITE TIMING WITH STRETCH= 1



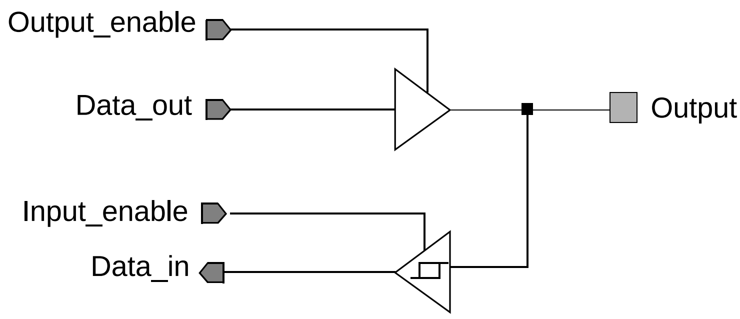


25 EXTERNAL AUX MEMORY WRITE TIMING WITH STRETCH= 2



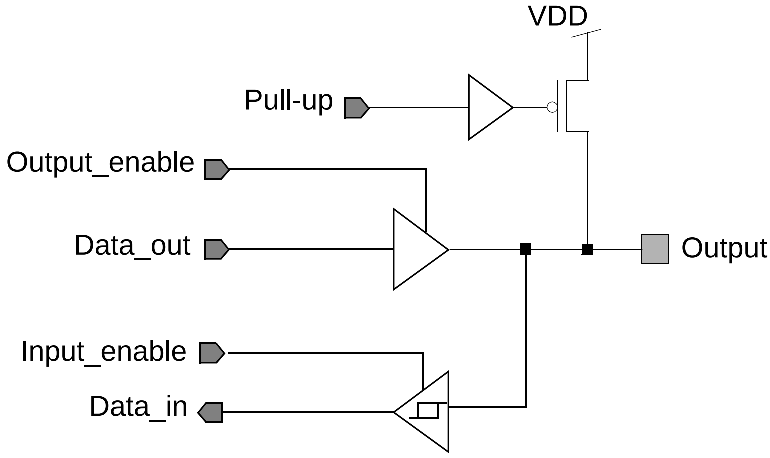
26 PIN CIRCUITS

26.1 Port 0 (P0.0 ~ P0.7) circuit (Bidirectional Input/Output)



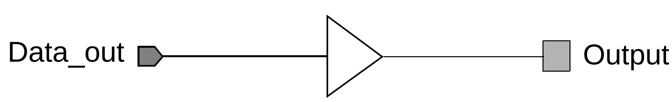
Port 0 pins are push-pull outputs. The output sinking capability is 4 mA (typ.). The sourcing capability is typically 200 µA.

26.2 Port 1 (P1.0 ~ P1.7), Port 2 (P2.0 ~ P2.7), Port 3 (P3.0 ~ P3.7) circuit (Bidirectional I/O, with weak Pull-up)

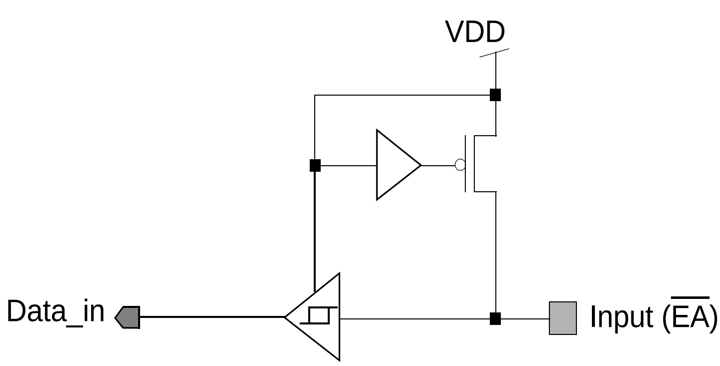


Pins of Port 1, Port 2, and Port 3 are push-pull outputs with weak internal pull-up. The output sinking capability is 4 mA (typ.). The typical value of the equivalent resistance of the pull-up PMOS is 15K ohm.

26.3 ALE and $\overline{PSEN}$ (Output)

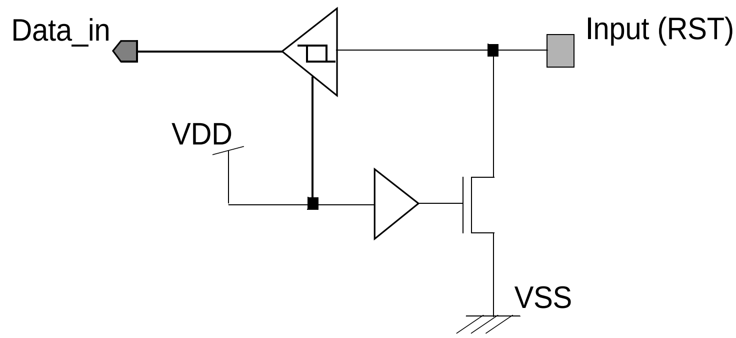


26.4 $\overline{EA}$ (Input)



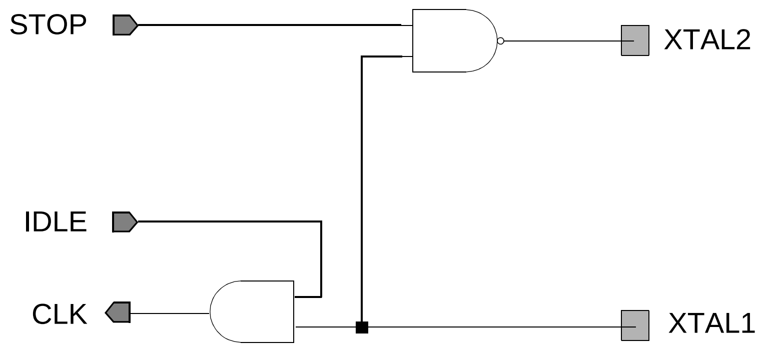
Note: This pin is weakly pulled up.

26.5 RST (Input)



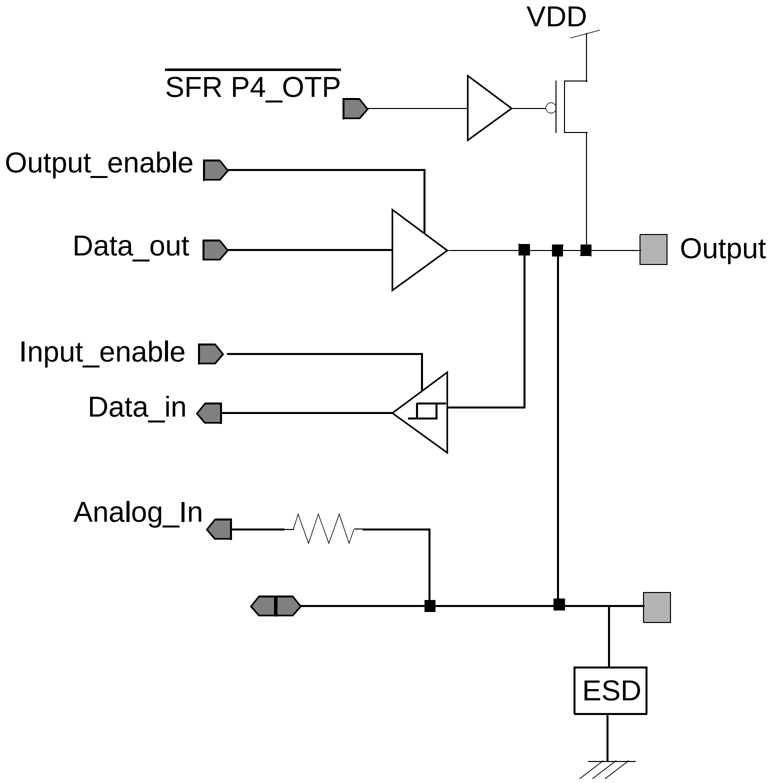
Note: This pin is weakly pulled down.

26.6 XTAL1, XTAL2



Please refer to Fig.35 for detail.

26.7 Port 4 (P4.0/ADC0, P4.1/ADC1, P4.2/ADC2, P4.3/ADC3)



Weak pull-up PMOS must be turned off when used as ADC input.

27 REDUCING ELECTROMAGNETIC EMISSION

There are two recommended ways to reduce chip's EMI emission: filtering and turning off ALE.

27.1 Filtering

Primary attention has been paid to the reduction of electromagnetic emission in the design of the STK6031. For example, the internal clock routing has been carefully arranged and internal decoupling capacitance has been added. However, in application, it is recommended that external capacitors should be connected across VDD and VSS pins. Lead length should be as short as possible. Ceramic chip capacitors are recommended (100 nF).

27.2 Turning off ALE

For applications that require no external memory or temporarily no external memory: the ALE output (pulses at a frequency of $\frac{1}{4} \times f_{OSC}$) can be disabled by setting CHIPCON.3=1 (bit 3 of SFR CHIPCON at SFR address BF hex); if disabled, no ALE pulse will occur. ALE pin will be weakly pulled high internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE (when external Data Memory is accessed).

Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal Program Memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, without regard to if bit 3 of SFR CHIPCON is set or not.

For detailed description of the SFR CHIPCON, please refer to Table 3 and Table 4.

28 INSTRUCTION SET

The STK6031's instruction set is binary-code-compatible with industrial standard 80C51. It consists of:

- 49 single byte,
- 45 two byte, and
- 17 three byte instructions.

A summary of the instruction set is given in Table 55, Table 56, Table 57, Table 58 and Table 59.

28.1 Addressing modes

Most instructions have a destination, source field that specifies the data type, addressing modes and operands involved. For all these instructions, except for MOVs, the destination operand is also the source operand (e.g. ADD A,R7).

There are five kinds of addressing modes:

- Register Addressing
  - R0 to R7 (4 banks)
  - A,B,C (bit), AB (2 bytes), DPTR (double byte)
- Direct Addressing
  - lower 128 bytes of internal main RAM (including the four R0 to R7 register banks)
  - Special Function Registers
  - 128 bits in a subset of the internal main RAM
  - 128 bits in a subset of the Special Function Registers
- Register-Indirect Addressing
  - internal main RAM (@R0, @R1, @SP [PUSH/POP])
  - internal auxiliary RAM (@R0, @R1, @DPTR)
  - external auxiliary RAM (@R0, @R1, @DPTR)
- Immediate Addressing
  - Program Memory (in-code 8 bit or 16 bit constant)
- Base-Register-plus-Index-Register-Indirect Addressing
  - Program Memory look-up table (@DPTR+A, @PC+A).

The first three addressing modes are usable for destination operands.

28.2 80C51 family instruction set

Table 54 Instructions that affect flag settings; note 1

INSTRUCTION	FLAG[2]		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X	X	
RRC	X		
RLC	X		
SETB C	1		
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C,/bit	X		
ORL C, bit	X		
ORL C,/bit	X		
MOV C, bit	X		
CJNE	X		

Note

1. Note that operations on SFR byte address 208 or bit addresses 209 to 215 (i.e. the PSW or bits in the PSW) will also affect flag settings.
2. X = dont care.

28.3 Instruction set description

For the description of the **Data Addressing Modes** and **Hexadecimal opcode cross-reference** see Table 59.

Table 55 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	2	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	2	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	2	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	2	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	2	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	2	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	2	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	2	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	3	A3
MUL	AB	Multiply A and B	1	5	A4
DIV	AB	Divide A by B	1	5	84
DA	A	Decimal adjust A	1	1	D4

Table 56 Instruction set: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	2	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	2	54
ANL	direct,A	AND A to direct byte	2	2	52
ANL	direct,#data	AND immediate data to direct byte	3	3	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	2	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	2	44
ORL	direct,A	OR A to direct byte	2	2	42
ORL	direct,#data	OR immediate data to direct byte	3	3	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	2	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	2	64
XRL	direct,A	Exclusive-OR A to direct byte	2	2	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 57 Instruction set: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	2	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	2	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	2	7*
MOV	direct,A	Move A to direct byte	2	2	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	3	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	2	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	3	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	3	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	3	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2 ~ 9	EB, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2 ~ 9	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2 ~ 9	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2 ~ 9	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	2	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 58 Instruction set: Boolean variable manipulation, Program flow control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	2	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	2	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	2	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	2	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Branching					
ACALL	addr11	Absolute subroutine call	2	3	•1
LCALL	addr16	Long subroutine call	3	4	12
RET		Return from subroutine	1	4	22
RETI		Return from interrupt	1	4	32
AJMP	addr11	Absolute jump	2	3	♦1
LJMP	addr16	Long jump	3	4	02
SJMP	rel	Short jump (relative address)	2	3	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	3	73
JZ	rel	Jump if A is zero	2	3	60
JNZ	rel	Jump if A is not zero	2	3	70
JC	rel	Jump if carry flag is set	2	3	40
JNC	rel	Jump if carry flag is not set	2	3	50
JB	bit,rel	Jump if direct bit is set	3	4	20
JNB	bit,rel	Jump if direct bit is not set	3	4	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	4	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	4	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	4	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	4	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	4	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	3	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	4	D5
NOP		No operation	1	1	00
All mnemonics are copyright © Intel Corporation 1980.					

Table 59 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 60 Instruction map

First hexadecimal character of opcode ↓ **← Second hexadecimal character of opcode →**

↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	1	MOV direct,Rr 0	1	2	3	4	5	6	7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	1	SUB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	1	MOV Rr,direct 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	1	CJNE Rr,#data,rel 0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	1	DJNZ Rr,rel 0	1	2	3	4	5	6	7

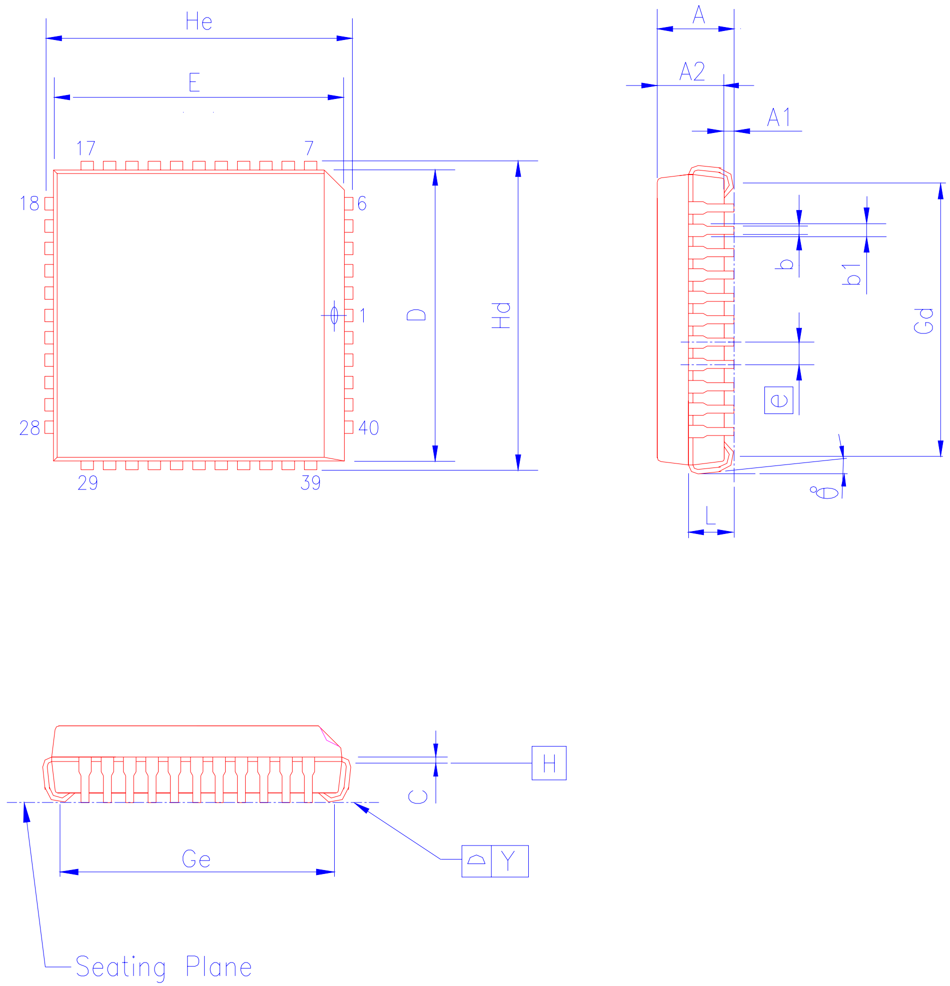
First hexadecimal character of opcode ← **Second hexadecimal character of opcode** →

↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri		CLR A	MOV A,direct [1]	MOV A,@Ri		MOV A,Rr							
			0	1			0	1	0	1	2	3	4	5	6	7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A		CPL A	MOV direct,A	MOV @Ri,A		MOV Rr,A							
			0	1			0	1	0	1	2	3	4	5	6	7

Note

1. MOV A, ACC is not a valid instruction.

29 PLCC44 PACKAGE OUTLINE DRAWING



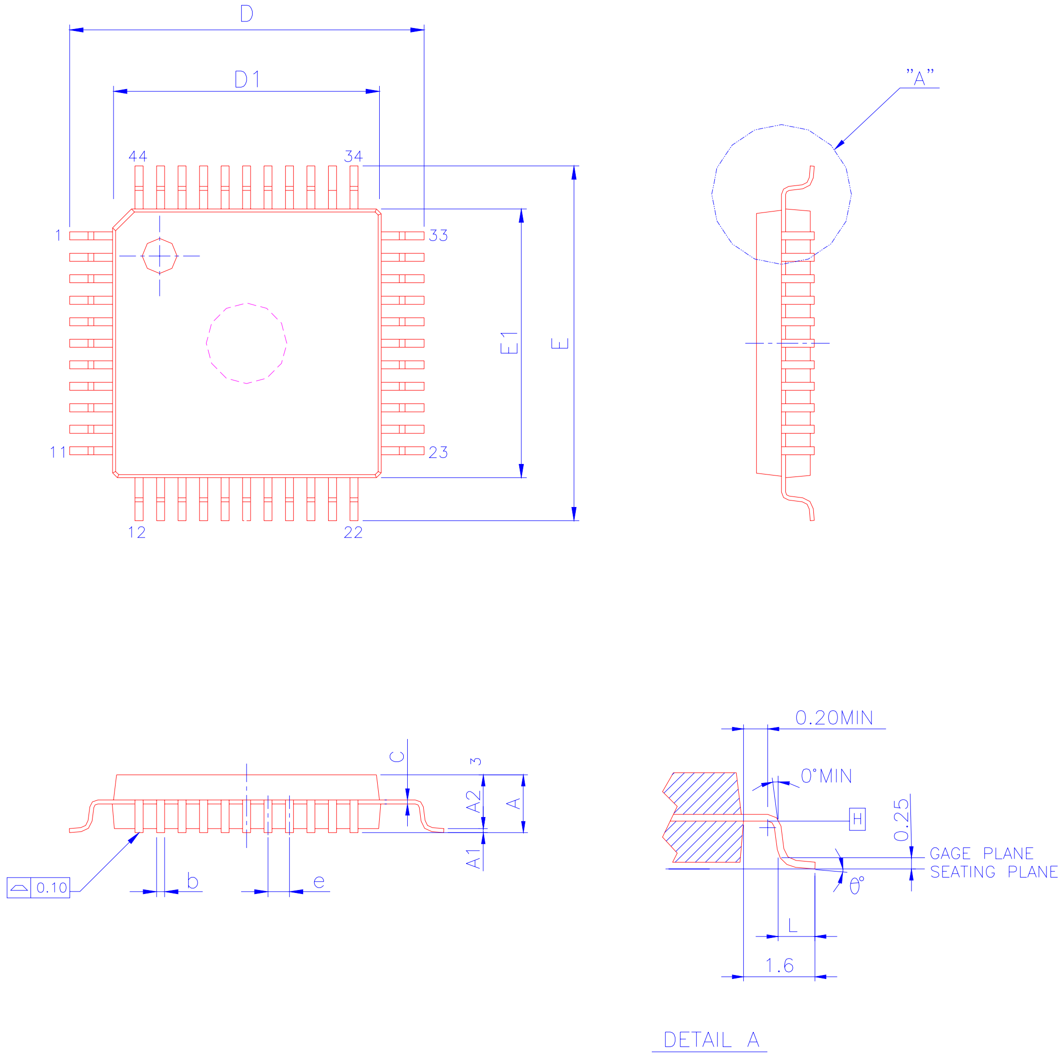
	SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
⚠1	A	0.165	–	0.180	4.191	–	4.572
	A1	0.020	–	–	0.508	–	–
⚠1	A2	0.147	–	0.158	3.734	–	4.013
	b1	0.026	0.028	0.032	0.660	0.711	0.813
⚠1	b	0.013	0.017	0.021	0.330	0.432	0.533
	c	0.007	0.010	0.013	0.178	0.254	0.330
⚠1	D	0.650	0.653	0.656	16.510	16.586	16.662
⚠1	E	0.650	0.653	0.656	16.510	16.586	16.662
	[e]	0.050 BSC			1.270 BSC		
	Gd	0.590	0.610	0.630	14.986	15.494	16.002
	Ge	0.590	0.610	0.630	14.986	15.494	16.002
	Hd	0.685	0.690	0.695	17.399	17.526	17.653
	He	0.685	0.690	0.695	17.399	17.526	17.653
	L	0.100	–	0.112	2.540	–	2.845
	Y	–	–	0.004	–	–	0.102

* *NOTE:*

1. JEDEC OUTLINE : MO-047 AC
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H] .
4. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION .

Fig.43 STK6031 PLCC44 Package Outline Drawing

30 QFP44 PACKAGE OUTLINE DRAWING



SYMBOLS	MIN.	NOM	MAX.
A	–	–	2.7
A1	0.25	–	0.50
A2	1.9	2.0	2.2
b	0.3 (TYP.)		
D	13.00	13.20	13.40
D1	9.9	10.00	10.10
E	13.00	13.20	13.40
E1	9.9	10.00	10.10
L	0.73	0.88	0.93
e	0.80 (TYP.)		
θ°	0	–	7
C	0.1	0.15	0.2

UNIT : mm

NOTES:

1.JEDEC OUTLINE:MO-108 AA-1

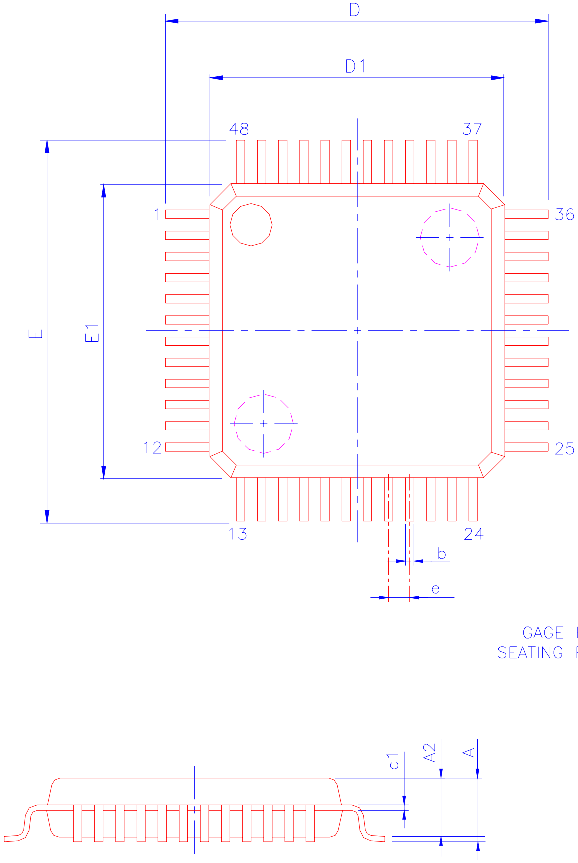
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

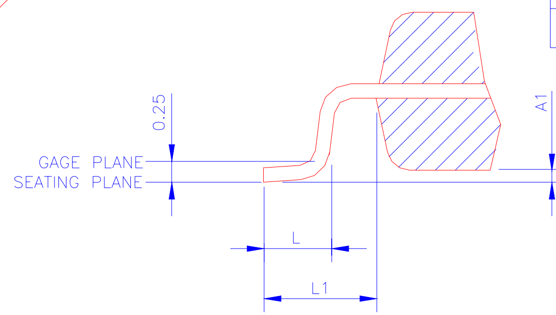
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

Fig.44 STK6031 QFP44 Package Outline Drawing

31 LQFP48 PACKAGE OUTLINE DRAWING





VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Fig.45 STK6031 LQFP48 Package Outline Drawing