RM48Lx40 16/32-Bit RISC Flash Microcontroller

1 RM48Lx40 16/32-Bit RISC Flash Microcontroller

1.1 Features

- High-Performance Microcontroller for Safety Critical Applications
  - Dual CPU's running in lockstep
  - ECC on flash and RAM interfaces
  - Built-In Self Test for CPU and on-chip RAMs
  - Error Signaling Module with Error Pin
  - Voltage and Clock Monitoring
- ARM® Cortex™ – R4F 32-bit RISC CPU
  - Efficient 1.6DMIPS/MHz with 8-stage pipeline
  - Floating-Point Unit with Single/Double Precision
  - 12-Region Memory Protection Unit
  - Open Architecture with 3rd Party Support
- Operating Conditions
  - Up to 200MHz System Clock
  - Core Supply Voltage (VCC): 1.2V nominal
  - I/O Supply Voltage (VCCIO): 3.3V nominal
- Integrated Memory
  - Up to 3MB Program Flash with ECC
  - Up to 256KB RAM with ECC
  - 64KB Flash for emulated EEPROM
- 16- bit External Memory Interface
- Common Platform Architecture
  - Consistent memory map across family
  - Real-Time Interrupt Timer (RTI) OS Timer
  - 96-channel Vectored Interrupt Module (VIM)
  - 2-channel Cyclic Redundancy Checker (CRC)
- Direct Memory Access (DMA) Controller
  - 16 Channels and 32 Control Packets
  - Parity protection for control packet RAM
  - DMA Accesses Protected by Dedicated MPU
- Frequency-Modulated Phase-Locked-Loop (FMPLL) with Built-In Slip Detector
- Separate Non-Modulating PLL
- IEEE 1149.1 JTAG, Boundary Scan and ARM CoreSight Components
- JTAG Security Module
- Trace and Calibration Capabilities
  - Embedded Trace Macrocell (ETM-R4)
  - Data Modification Module (DMM)
  - RAM Trace Port (RTP)
  - Parameter Overlay Module (POM)
- Multiple Communication Interfaces
  - 10/100 Mbps Ethernet MAC (EMAC)
    - IEEE 802.3 compliant (3.3V-I/O only)
    - Supports MII and MDIO
  - Three CAN Controllers (DCAN)
    - 64 mailboxes with parity protection each
    - Compliant to CAN protocol version 2.0B
  - Inter-Integrated Circuit (I^2C)
  - Three Multi-buffered Serial Peripheral Interfaces (MibSPI)
    - 128 Words with Parity Protection each
  - Two Standard Serial Peripheral Interfaces (SPI)
  - Local Interconnect Network Interface (LIN) Controller
    - Compliant to LIN protocol version 2.1
  - Standard Serial Communication Interface (SCI)
- Two High-End Timer Modules (N2HET)
  - N2HET1: 32 programmable channels
  - N2HET2: 20 programmable channels
  - 160 Word Instruction RAM with parity protection each
  - Each includes Hardware Angle Generator
  - Dedicated Transfer Unit for each N2HET (HTU)
- Two 10/12-bit Multi-Buffered ADC Modules
  - ADC1: 24 channels
  - ADC2: 16 channels
  - 16 shared channels
  - 64 result buffers with parity protection each
- Packages
  - 144-pin Quad Flatpack (PGE) [Green]
  - 337-Ball Grid Array (ZWT) [Green]

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1.2 Applications

- **Industrial Safety Applications**
  - **Industrial Automation**
  - **Safe PLC's (Programmable Logic Controllers)**
  - **Power Generation and Distribution**
  - **Turbines and Windmills**
  - **Elevators and Escalators**
- **Medical Applications**
  - **Ventilators**
  - **Defibrillators**
  - **Infusion and Insulin pumps**
  - **Radiation therapy**
  - **Robotic surgery**

1.3 Description

The RM48Lx40 is a high performance microcontroller family for safety systems. The safety architecture includes Dual CPUs in lockstep, CPU and Memory Built-In Self Test (BIST) logic, ECC on both the Flash and the data SRAM, parity on peripheral memories, and loop back capability on peripheral IOs.

The RM48Lx40 integrates the ARM® Cortex™-R4F Floating Point CPU which offers an efficient 1.6 DMIPS/MHz, and has configurations which can run up to 200MHz providing up to 320 DMIPS. The device supports the little-endian [LE32] format.

The RM48Lx40 has up to 3MB integrated Flash and up to 256KB data RAM configurations with single bit error correction and double bit error detection. The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3V supply input (same level as I/O supply) for all read, program and erase operations. When in pipeline mode, the flash operates with a system clock frequency of up to 200MHz. The SRAM supports single-cycle read/write accesses in byte, halfword, and word modes.

The RM48Lx40 device features peripherals for real-time control-based applications, including two Next Generation High End Timer (N2HET) timing coprocessors with up to 44 total IO terminals and a 12-bit Analog-to-Digital converter supporting up to 24 inputs.

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. A High End Timer Transfer Unit (HET-TU) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HET-TU.

The device has two 12-bit-resolution MibADCs with 24 total channels and 64 words of parity protected buffer RAM each. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. Sixteen channels are shared between the two MibADCs. There are three separate groupings. Each sequence can be converted once when triggered or configured for continuous conversion mode.

The device has multiple communication interfaces: three MibSPIs, up to two SPIs, one LIN, one SCI, three DCANs, one I^2C, one Ethernet. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The LIN supports the Local Interconnect standard 2.0 and can be used as a UART in full-duplex mode using the standard Non-Return-to-Zero (NRZ) format. The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring. The Ethernet module supports MII and MDIO interfaces.

The I2C module is a multi-master communication module providing an interface between the microcontroller and an I2C compatible device via the I2C serial bus. The I2C supports both 100 Kbps and 400 Kbps speeds.

The frequency-modulated phase-locked loop (FMPLL) clock module is used to multiply the external frequency reference to a higher frequency for internal use. The FMPLL provides one of the seven possible clock source inputs to the global clock module (GCM). The GCM module manages the mapping between the available clock sources and the device clock domains.

The device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock on the ECLK pin/ball. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency. This low frequency output can be monitored externally as an indicator of the device operating frequency.

The Direct Memory Access Controller (DMA) has 16 channels, 32 control packets and parity protection on its memory. A Memory Protection Unit (MPU) is built into the DMA to protect memory against erroneous transfers.

The Error Signaling Module (ESM) monitors all device errors and determines whether an interrupt or external Error pin/ball is triggered when a fault is detected. The nERROR can be monitored externally as an indicator of a fault condition in the microcontroller.

The External Memory Interface (EMIF) provides a memory extension to asynchronous and synchronous memories or other slave devices.

Several interfaces are implemented to enhance the debugging capabilities of application code. In addition to the built in ARM Cortex™-R4F CoreSight™ debug features. An External Trace Macrocell (ETM) provides instruction and data trace of program execution. For instrumentation purposes, a RAM Trace Port Module (RTP) is implemented to support high-speed tracing of RAM and peripheral accesses by the CPU or any other master. A Data Modification Module (DMM) gives the ability to write external data into the device memory. Both the RTP and DMM have no or only minimum impact on the program execution time of the application code. A Parameter Overlay Module (POM) can re-route Flash accesses to internal memory or to the EMIF, thus avoiding the re-programming steps necessary for parameter updates in Flash.

With integrated safety features and a wide choice of communication and control peripherals, the RM48Lx40 is an ideal solution for high performance real time control applications with safety critical requirements.

1.4 Functional Block Diagram

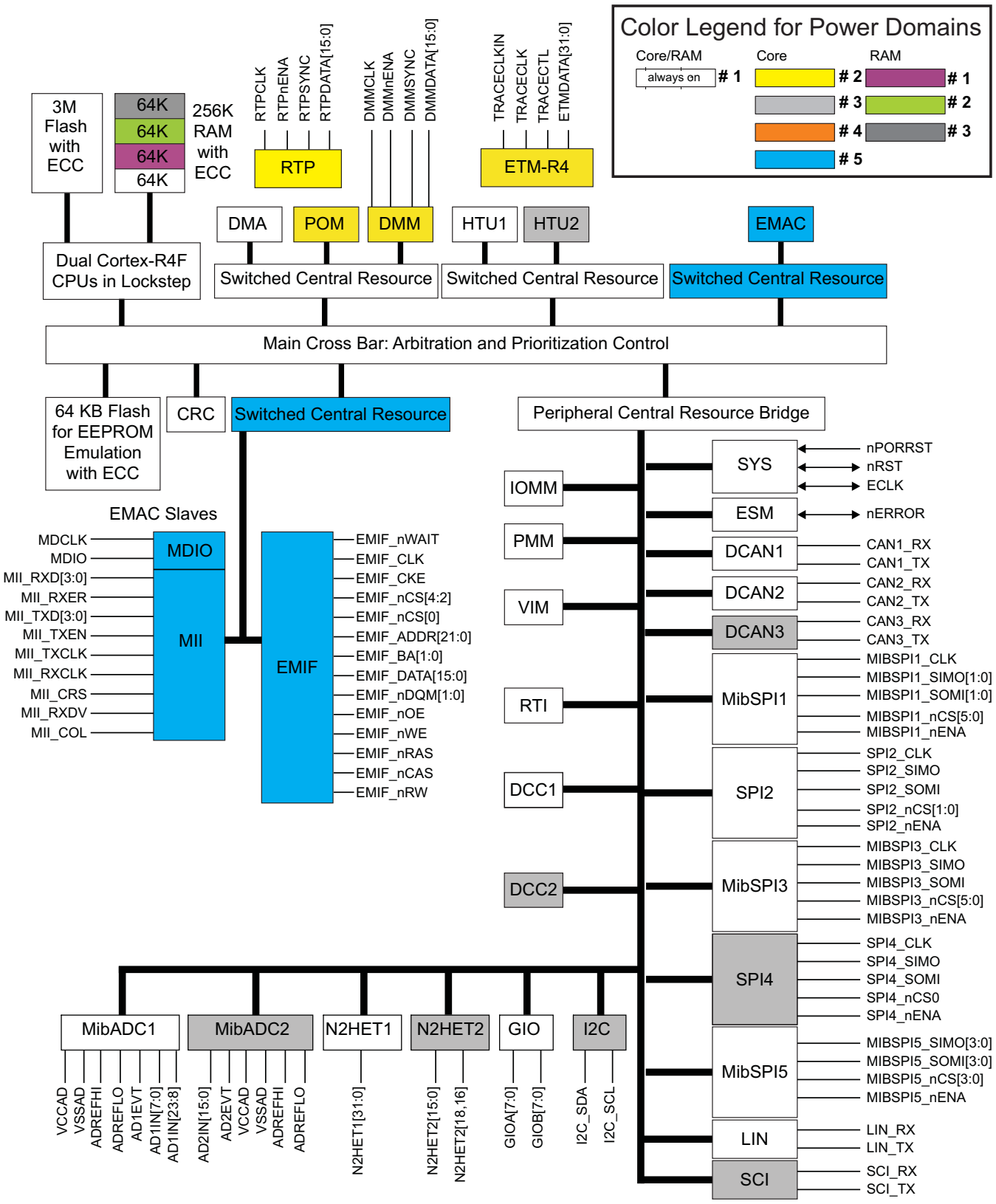

Figure 1-1. Functional Block Diagram

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1.1 Device Configuration

1.1.1 Device and Development-Support Tool Nomenclature

The figure below illustrates the numbering and symbol nomenclature for the RM48Lx40 .

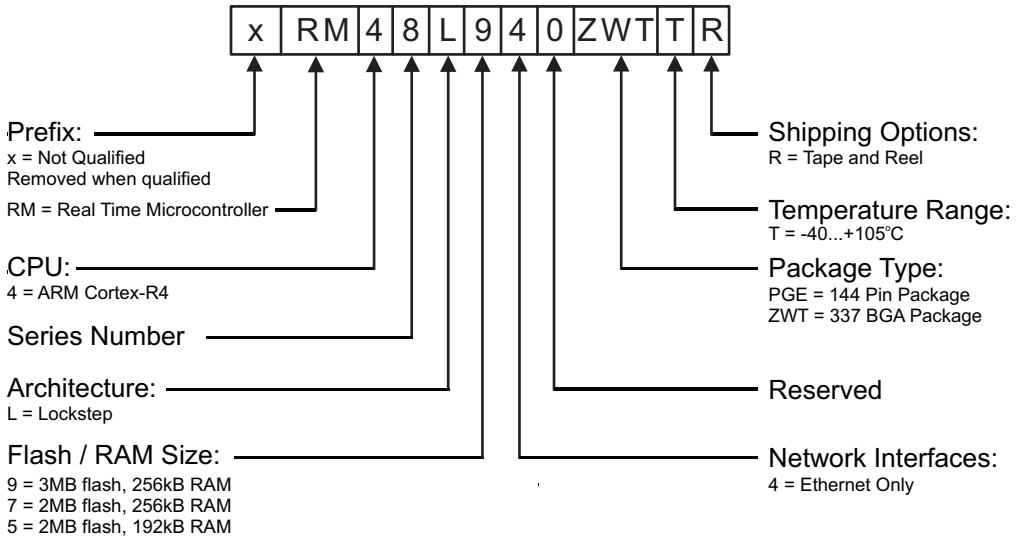

Figure 1-1. RM48x Device Numbering Conventions

1.1.2 Orderable Part Numbers

Table 1-1. Orderable Part Numbers

Orderable Part #	Part #	Flash	RAM	EMAC(1)	USB(2)
RM48L540PGET	RM48L540	2MB	192kB	Yes	-
RM48L540ZWTT	RM48L540	2MB	192kB	Yes	-
RM48L740PGET	RM48L740	2MB	256kB	Yes	-
RM48L740ZWTT	RM48L740	2MB	256kB	Yes	-
RM48L940PGET	RM48L940	3MB	256kB	Yes	-
RM48L940ZWTT	RM48L940	3MB	256kB	Yes	-

(1) 10/100
(2) 2 host ports, or 1 host port + 1 device port

1.1.3 Device Identification

1.1.3.1 Device Identification Code Register

The device identification code register identifies several aspects of the device including the silicon version. The details of the device identification code register are shown in Table 1-2. The device identification code register value for this device is:

- Rev 0 = 0x802AAD05

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Figure 1-2. Device ID Bit Allocation Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CP-15	UNIQUE ID														TECH
R-1	R-00000000010101														R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TECH			I/O VOLTAGE	PERIPH PARITY	FLASH ECC		RAM ECC	VERSION					1	0	1
R-101			R-0	R-1	R-10		R-1	R-00000					R-1	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

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Table 1-2. Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31	CP15		Indicates the presence of coprocessor 15
		1	CP15 present
30-17	UNIQUE ID	10101	Silicon version (revision) bits. This bitfield holds a unique number for a dedicated device configuration (die).
16-13	TECH		Process technology on which the device is manufactured.
		0101	F021
12	I/O VOLTAGE		I/O voltage of the device.
		0	I/O are 3.3v
11	PERIPHERAL PARITY		Peripheral Parity
		1	Parity on peripheral memories
10-9	FLASH ECC		Flash ECC
		10	Program memory with ECC
8	RAM ECC		Indicates if RAM memory ECC is present.
		1	ECC implemented
7-3	REVISION		Revision of the Device.
2-0	101		The platform family ID is always 0b101

1.1.3.2 Die Identification Registers

The four die ID registers at addresses 0xFFFFE1F0, 0xFFFFE1F4, 0xFFFFE1F8 and FFFFE1FC form a 128-bit dieid with the information as shown in Table Table 1-3.

Table 1-3. Die-ID Registers

Item	# of Bits	Bit Location
X Coord. on Wafer	8	7..0
Y Coord. on Wafer	8	15..8
Wafer #	6	21..16
Lot #	24	45..22
Reserved	82	127..46

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2 Device Package and Terminal Functions

2.2 PGE QFP Package Pinout (144-Pin)

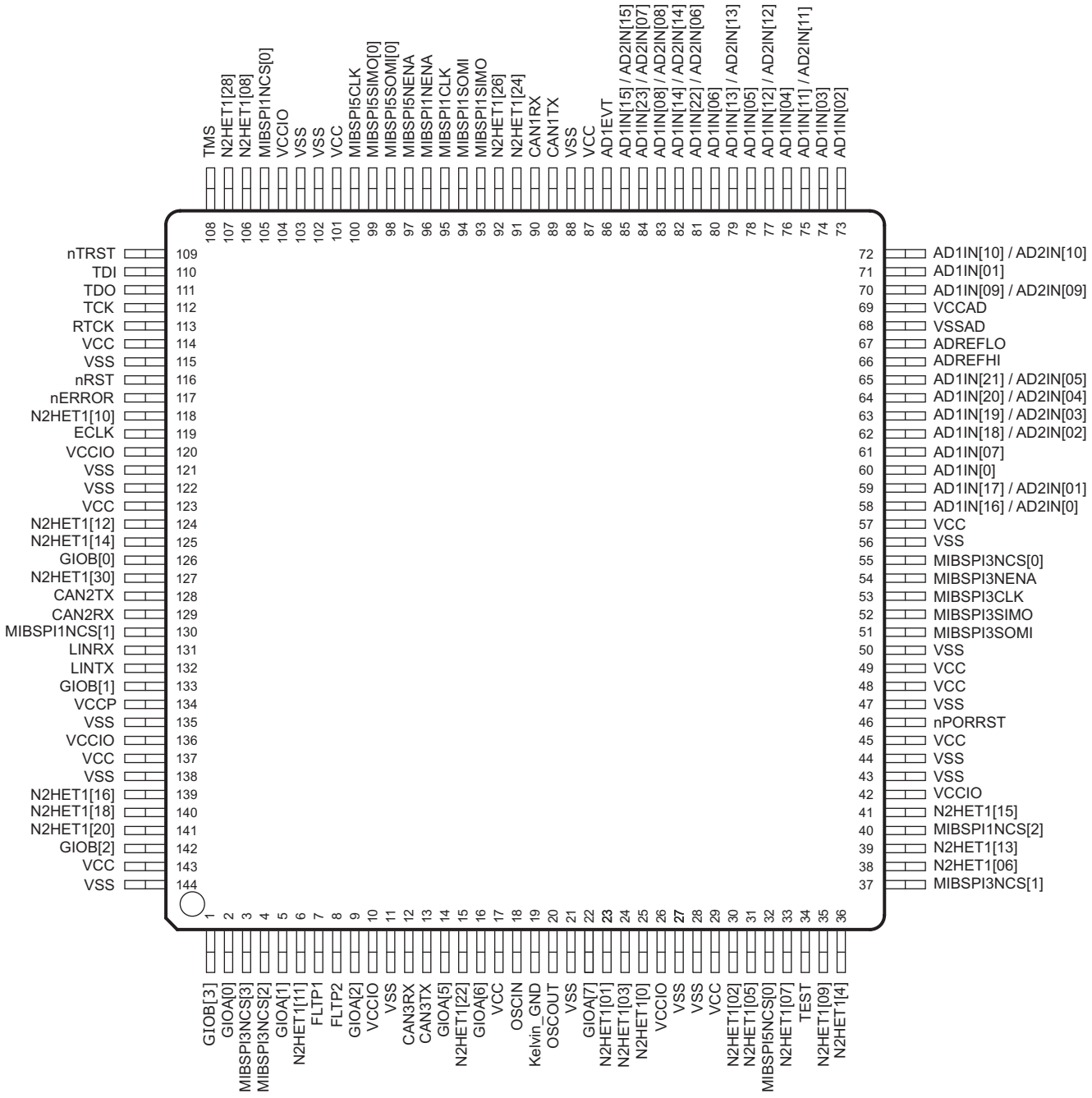

Figure 2-3. PGE QFP Package Pinout (144-Pin)

Note: Pins can have multiplexed functions. Only the default function is depicted in above diagram.

2.3 ZWT BGA Package Ball-Map (337 Ball Grid Array)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	
19	VSS	VSS	TMS	N2HET1 [10]	MIBSPI5 NCS[0]	MIBSPI1 SIMO	MIBSPI1 NENA	MIBSPI5 CLK	MIBSPI5 SIMO[0]	N2HET1 [28]	DMM_ DATA[0]	CAN3RX	AD1EVT	AD1IN[15] / AD2IN[15]	AD1IN[22] / AD2IN[06]	AD1IN [06]	AD1IN[11] / AD2IN[11]	VSSAD	VSSAD	19
18	VSS	TCK	TDO	nTRST	N2HET1 [08]	MIBSPI1 CLK	MIBSPI1 SOMI	MIBSPI5 NENA	MIBSPI5 SOMI[0]	N2HET1 [0]	DMM_ DATA[1]	CAN3TX	NC	AD1IN[08] / AD2IN[08]	AD1IN[14] / AD2IN[14]	AD1IN[13] / AD2IN[13]	AD1IN [04]	AD1IN [02]	VSSAD	18
17	TDI	RST	EMIF_ ADDR[21]	EMIF_ nWE	MIBSPI5 SOMI[1]	DMM_ CLK	MIBSPI5 SIMO[3]	MIBSPI5 SIMO[2]	N2HET1 [31]	EMIF_ nCS[3]	EMIF_ nCS[2]	EMIF_ nCS[4]	EMIF_ nCS[0]	NC	AD1IN [05]	AD1IN [03]	AD1IN[10] / AD2IN[10]	AD1IN [01]	AD1IN[09] / AD2IN[09]	17
16	RTCK	NC	EMIF_ ADDR[20]	EMIF_ BA[1]	MIBSPI5 SIMO[1]	DMM_ NENA	MIBSPI5 SOMI[3]	MIBSPI5 SOMI[2]	DMM_ SYNC	NC	NC	NC	NC	NC	AD1IN[23] / AD2IN[07]	AD1IN[12] / AD2IN[12]	AD1IN[19] / AD2IN[03]	ADREFLO	VSSAD	16
15	NC	NC	EMIF_ ADDR[19]	EMIF_ ADDR[18]	ETM DATA[06]	ETM DATA[05]	ETM DATA[04]	ETM DATA[03]	ETM DATA[02]	ETM DATA[16]	ETM DATA[17]	ETM DATA[18]	ETM DATA[19]	NC	NC	AD1IN[21] / AD2IN[05]	AD1IN[20] / AD2IN[04]	ADREFHI	VCCAD	15
14	N2HET1 [26]	nERROR	EMIF_ ADDR[17]	EMIF_ ADDR[16]	ETM DATA[07]	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	VCCIO	VCCIO	VCCIO	NC	NC	AD1IN[18] / AD2IN[02]	AD1IN [07]	AD1IN [0]	14
13	N2HET1 [17]	N2HET1 [19]	EMIF_ ADDR[15]	NC	ETM DATA[12]	VCCIO								VCCIO	ETM DATA[01]	NC	AD1IN[17] / AD2IN[01]	AD1IN[16] / AD2IN[0]	NC	13
12	ECLK	N2HET1 [04]	EMIF_ ADDR[14]	NC	ETM DATA[13]	VCCIO		VSS	VSS	VCC	VSS	VSS		VCCIO	ETM DATA[0]	MIBSPI5 NCS[3]	NC	NC	NC	12
11	N2HET1 [14]	N2HET1 [30]	EMIF_ ADDR[13]	NC	ETM DATA[14]	VCCIO		VSS	VSS	VSS	VSS	VSS		VCCPLL	ETME TRACE CTL	NC	NC	NC	NC	11
10	CAN1TX	CAN1RX	EMIF_ ADDR[12]	NC	ETM DATA[15]	VCC		VCC	VSS	VSS	VSS	VCC		VCC	ETM TRACE CLKOUT	NC	NC	MIBSPI3 NCS[0]	GIOB[3]	10
9	N2HET1 [27]	NC	EMIF_ ADDR[11]	NC	ETM DATA[08]	VCC		VSS	VSS	VSS	VSS	VSS		VCCIO	ETM TRACE CLKIN	NC	NC	MIBSPI3 CLK	MIBSPI3 NENA	9
8	NC	NC	EMIF_ ADDR[10]	NC	ETM DATA[09]	VCCP		VSS	VSS	VCC	VSS	VSS		VCCIO	ETM DATA[31]	NC	NC	MIBSPI3 SOMI	MIBSPI3 SIMO	8
7	LINRX	LINTX	EMIF_ ADDR[9]	NC	ETM DATA[10]	VCCIO								VCCIO	ETM DATA[30]	NC	NC	N2HET1 [09]	nPORRST	7
6	GIOA[4]	MIBSPI5 NCS[1]	EMIF_ ADDR[8]	NC	ETM DATA[11]	VCCIO	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	VCCIO	VCCIO	ETM DATA[29]	NC	NC	N2HET1 [05]	MIBSPI5 NCS[2]	6
5	GIOA[0]	GIOA[5]	EMIF_ ADDR[7]	EMIF_ ADDR[1]	ETM DATA[20]	ETM DATA[21]	ETM DATA[22]	FLTP2	FLTP1	ETM DATA[23]	ETM DATA[24]	ETM DATA[25]	ETM DATA[26]	ETM DATA[27]	ETM DATA[28]	NC	NC	MIBSPI3 NCS[1]	N2HET1 [02]	5
4	N2HET1 [16]	N2HET1 [12]	EMIF_ ADDR[6]	EMIF_ ADDR[0]	NC	NC	NC	N2HET1 [21]	N2HET1 [23]	NC]	NC	NC	NC	NC	EMIF_ nCAS	NC	NC	NC	NC	4
3	N2HET1 [29]	N2HET1 [22]	MIBSPI3 NCS[3]	SPI2 NENA	N2HET1 [11]	MIBSPI1 NCS[1]	MIBSPI1 NCS[2]	GIOA[6]	MIBSPI1 NCS[3]	EMIF_ CLK	EMIF_ CKE	NH2ET1 [25]	SPI2 NCS[0]	EMIF_ nWAIT	EMIF_ nRAS	NC	NC	NC	N2HET1 [06]	3
2	VSS	MIBSPI3 NCS[2]	GIOA[1]	SPI2 SOMI	SPI2 CLK	GIOB[2]	GIOB[5]	CAN2TX	GIOB[6]	GIOB[1]	KELVIN_ GND	GIOB[0]	N2HET1 [13]	N2HET1 [20]	MIBSPI1 NCS[0]	NC	TEST	N2HET1 [01]	VSS	2
1	VSS	VSS	GIOA[2]	SPI2 SIMO	GIOA[3]	GIOB[7]	GIOB[4]	CAN2RX	N2HET1 [18]	OSCIN	OSCOUT	GIOA[7]	N2HET1 [15]	N2HET1 [24]	NC	N2HET1 [07]	N2HET1 [03]	VSS	VSS	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	

Figure 2-4. ZWT Package Pinout. Top View

Note: Balls can have multiplexed functions. Only the default function is depicted in above diagram, except for the EMIF signals that are multiplexed with ETM signals.

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2.4 Terminal Functions

Section 2.4.1 and Section 2.4.2 identify the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin/ball type (Input, Output, IO, Power or Ground), whether the pin/ball has any internal pullup/pulldown, whether the pin/ball can be configured as a GIO, and a functional pin/ball description. The first signal name listed is the primary function for that terminal. The signal name in Bold is the function being described. Refer to the I/O Multiplexing Module (IOMM) User Guide for information on how to select between different multiplexed functions.

NOTE

All I/O signals except nRST are configured as inputs while nPORRST is low and immediately after nPORRST goes High.

All output-only signals are configured as inputs while nPORRST is low, and are configured as outputs immediately after nPORRST goes High.

While nPORRST is low, the input buffers are disabled, and the output buffers are tri-stated.

2.4.1 PGE Package

2.4.1.1 Multi-Buffered Analog-to-Digital Converters (MibADC)

Table 2-4. PGE Multi-Buffered Analog-to-Digital Converters (MibADC1, MibADC2)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
ADREFHI(1)	66	Input	-	-	ADC high reference supply
ADREFLO(1)	67	Input			ADC low reference supply
VCCAD(1)	69	Power			Operating supply for ADC
VSSAD(1)	68	Ground			
AD1EVT/MII_RX_ER	86	Input	Pull Down	Programmable, 20uA	ADC1 event trigger input, or GIO
MIBSPI3NCS[0]/**AD2EVT**	55	I/O	Pull Up	Programmable, 20uA	ADC2 event trigger input, or GIO
AD1IN[0]	60	Input	-	-	ADC1 analog input
AD1IN[01]	71				
AD1IN[02]	73				
AD1IN[03]	74				
AD1IN[04]	76				
AD1IN[05]	78				
AD1IN[06]	80				
AD1IN[07]	61				

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.

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Table 2-4. PGE Multi-Buffered Analog-to-Digital Converters (MibADC1, MibADC2) (continued)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
AD1IN[08] / AD2IN[08]	83	Input	-	-	ADC1/ADC2 shared analog inputs
AD1IN[09] / AD2IN[09]	70				
AD1IN[10] / AD2IN[10]	72				
AD1IN[11] / AD2IN[11]	75				
AD1IN[12] / AD2IN[12]	77				
AD1IN[13] / AD2IN[13]	79				
AD1IN[14] / AD2IN[14]	82				
AD1IN[15] / AD2IN[15]	85				
AD1IN[16] / AD2IN[0]	58				
AD1IN[17] / AD2IN[01]	59				
AD1IN[18] / AD2IN[02]	62				
AD1IN[19] / AD2IN[03]	63				
AD1IN[20] / AD2IN[04]	64				
AD1IN[21] / AD2IN[05]	65				
AD1IN[22] / AD2IN[06]	81				
AD1IN[23] / AD2IN[07]	84				

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2.4.1.2 Enhanced High-End Timer Modules (N2HET)

Table 2-5. PGE Enhanced High-End Timer Modules (N2HET)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
N2HET1[0]/SPI4CLK	25	I/O	Pull Down	Programmable, 20uA	N2HET1 time input capture or output compare, or GIO. Each terminal has a suppression filter that ignores input pulses smaller than a programmable duration.
N2HET1[01]/SPI4NENA/N2HET2[8]	23				
N2HET1[02]/SPI4SIMO	30				
N2HET1[03]/SPI4NCS[0]/N2HET2[10]	24				
N2HET1[04]	36				
N2HET1[05]/SPI4SOMI/N2HET2[12]	31				
N2HET1[06]/SCIRX	38				
N2HET1[07]/N2HET2[14]	33				
N2HET1[08]/MIBSPI1SIMO[1]/MII_TXD[3]/	106				
N2HET1[09]/N2HET2[16]	35				
N2HET1[10]/MII_TX_CLK/MII_TX_AVCLK4	118				
N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]	6				
N2HET1[12]/MII_CRS	124				
N2HET1[13]/SCITX	39				
N2HET1[14]	125				
N2HET1[15]/MIBSPI1NCS[4]	41				
N2HET1[16]	139				
MIBSPI1NCS[1]/**N2HET1[17]**/MII_COL	130				
N2HET1[18]	140				
MIBSPI1NCS[2]/**N2HET1[19]**/MDIO	40				
N2HET1[20]	141				
N2HET1[22]	15				
MIBSPI1NENA/**N2HET1[23]**/MII_RXD[2]	96				
N2HET1[24]/MIBSPI1NCS[5]/MII_RXD[0]	91				
MIBSPI3NCS[1]/**N2HET1[25]**/MDCLK	37				
N2HET1[26]/MII_RXD[1]	92				
MIBSPI3NCS[2]/I2C_SDA/**N2HET1[27]**	4				
N2HET1[28]/MII_RXCLK/MII_RX_AVCLK4	107				
MIBSPI3NCS[3]/I2C_SCL/**N2HET1[29]**	3				
N2HET1[30]/MII_RX_DV	127				
MIBSPI3NENA/MIBSPI3NCS[5]/**N2HET1[31]**	54				
GIOA[2]/**N2HET2[0]**	9	I/O	Pull Down	Programmable, 20uA	N2HET2 time input capture or output compare, or GIO Each terminal has a suppression filter that ignores input pulses smaller than a programmable duration.
GIOA[6]/**N2HET2[4]**	16				
GIOA[7]/**N2HET2[6]**	22				
N2HET1[01]/SPI4NENA/**N2HET2[8]**	23				
N2HET1[03]/SPI4NCS[0]/**N2HET2[10]**	24				
N2HET1[05]/SPI4SOMI/**N2HET2[12]**	31				
N2HET1[07]/**N2HET2[14]**	33				
N2HET1[09]/**N2HET2[16]**	35				
N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]**	6				

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2.4.1.3 General-Purpose Input / Output (GIO)

Table 2-6. PGE General-Purpose Input / Output (GIO)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
GIOA[0]	2	I/O	Pull Down	Programmable, 20uA	General-purpose I/O. All GIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges.
GIOA[1]	5				
GIOA[2]/N2HET2[0]	9				
GIOA[5]/EXTCLKIN	14				
GIOA[6]/N2HET2[4]	16				
GIOA[7]/N2HET2[6]	22				
GIOB[0]	126				
GIOB[1]	133				
GIOB[2]	142				
GIOB[3]	1				

2.4.1.4 Controller Area Network Controllers (DCAN)

Table 2-7. PGE Controller Area Network Controllers (DCAN)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
CAN1RX	90	I/O	Pull Up	Programmable, 20uA	CAN1 receive, or GIO
CAN1TX	89				CAN1 transmit, or GIO
CAN2RX	129				CAN2 receive, or GIO
CAN2TX	128				CAN2 transmit, or GIO
CAN3RX	12				CAN3 receive, or GIO
CAN3TX	13				CAN3 transmit, or GIO

2.4.1.5 Local Interconnect Network Interface Module (LIN)

Table 2-8. PGE Local Interconnect Network Interface Module (LIN)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
LINRX	131	I/O	Pull Up	Programmable, 20uA	LIN receive, or GIO
LINTX	132				LIN transmit, or GIO

2.4.1.6 Standard Serial Communication Interface (SCI)

Table 2-9. PGE Standard Serial Communication Interface (SCI)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
N2HET1[06]/**SCIRX**	38	I/O	Pull Down	Programmable, 20uA	SCI receive, or GIO
N2HET1[13]/**SCITX**	39				SCI transmit, or GIO

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2.4.1.7 Inter-Integrated Circuit Interface Module (I2C)

Table 2-10. PGE Inter-Integrated Circuit Interface Module (I2C)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27]	4	I/O	Pull Up	Programmable, 20uA	I2C serial data, or GIO
MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29]	3				I2C serial clock, or GIO

2.4.1.8 Standard Serial Peripheral Interface (SPI)

Table 2-11. PGE Standard Serial Peripheral Interface (SPI)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
N2HET1[0]/**SPI4CLK**	25	I/O	Pull Down	Programmable, 20uA	SPI4 clock, or GIO
N2HET1[03]/**SPI4NCS[0]**/N2HET2[10]	24				SPI4 chip select, or GIO
N2HET1[01]/**SPI4NENA**/N2HET2[8]	23				SPI4 enable, or GIO
N2HET1[02]/**SPI4SIMO**	30				SPI4 slave-input master-output, or GIO
N2HET1[05]/**SPI4SOMI**/N2HET2[12]	31				SPI4 slave-output master-input, or GIO

2.4.1.9 Multi-Buffered Serial Peripheral Interface Modules (MibSPI)

Table 2-12. PGE Multi-Buffered Serial Peripheral Interface Modules (MibSPI)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI1CLK	95	I/O	Pull Up	Programmable, 20uA	MibSPI1 clock, or GIO
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/MII_TXD[2]	105				MibSPI1 chip select, or GIO
MIBSPI1NCS[1]/N2HET1[17]/MII_COL	130				
MIBSPI1NCS[2]/N2HET1[19]/MDIO	40				
N2HET1[15]/**MIBSPI1NCS[4]**	41		Pull Down	Programmable, 20uA	MibSPI1 chip select, or GIO
N2HET1[24]/**MIBSPI1NCS[5]**/MII_RXD[0]	91				
MIBSPI1NENA/N2HET1[23]/MII_RXD[2]	96		Pull Up	Programmable, 20uA	MibSPI1 enable, or GIO
MIBSPI1SIMO	93				MibSPI1 slave-in master-out, or GIO
N2HET1[08]/**MIBSPI1SIMO[1]**/MII_TXD[3]	106		Pull Down	Programmable, 20uA	MibSPI1 slave-in master-out, or GIO
MIBSPI1SOMI	94		Pull Up	Programmable, 20uA	MibSPI1 slave-out master-in, or GIO
MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/MII_TXD[2]	105				

Table 2-12. PGE Multi-Buffered Serial Peripheral Interface Modules (MibSPI) (continued)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI3CLK	53	I/O	Pull Up	Programmable, 20uA	MibSPI3 clock, or GIO
MIBSPI3NCS[0]/AD2EVT/GIOB[2]	55				MibSPI3 chip select, or GIO
MIBSPI3NCS[1]/N2HET1[25]/MDCLK	37				
MIBSPI3NCS[2]/I2C_SDA/N2HET1[27]	4				
MIBSPI3NCS[3]/I2C_SCL/N2HET1[29]	3				
N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18]	6		Pull Up	Programmable, 20uA	MibSPI3 chip select, or GIO
MIBSPI3NENA /**MIBSPI3NCS[5]**/N2HET1[31]	54		Pull Up	Programmable, 20uA	MibSPI3 chip select, or GIO
MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]	54				MibSPI3 enable, or GIO
MIBSPI3SIMO	52				MibSPI3 slave-in master-out, or GIO
MIBSPI3SOMI	51				MibSPI3 slave-out master-in, or GIO
MIBSPI5CLK/MII_TXEN	100	I/O	Pull Up	Programmable, 20uA	MibSPI5 clock, or GIO
MIBSPI5NCS[0]	32				MibSPI5 chip select, or GIO
MIBSPI5NENA/MII_RXD[3]	97				MibSPI5 enable, or GIO
MIBSPI5SIMO[0]/MII_TXD[1]	99				MibSPI5 slave-in master-out, or GIO
MIBSPI5SOMI[0]/MII_TXD[0]	98				MibSPI5 slave-out master-in, or GIO

2.4.1.10 Ethernet Controller

Table 2-13. PGE Ethernet Controller: MDIO Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI3NCS[1]/N2HET1[25]/**MDCLK**	37	Output	Pull Up	-	Serial clock output
MIBSPI1NCS[2]/N2HET1[19]/**MDIO**	40	I/O	Pull Up	Fixed, 20uA	Serial data input/output

Table 2-14. PGE Ethernet Controller: Media Independent Interface (MII)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI1NCS[1]/N2HET1[17]/**MII_COL**	130	Input	Pull Up	-	Collision detect
N2HET1[12]/**MII_CRS**	124		Pull Down	Fixed, 20uA	Carrier sense and receive valid
N2HET1[28]/MII_RXCLK/**MII_RX_AVCLK4**	107	I/O	Pull Down	-	MII output receive clock
N2HET1[30]/**MII_RX_DV**	127	Input	Pull Down	Fixed, 20uA	Received data valid
AD1EVT/**MII_RX_ER**	86				Receive error
N2HET1[28]/**MII_RX_CLK**/MII_RX_AVCLK4	107	I/O			Receive clock
N2HET1[24]/MIBSPI1NCS[5]/**MII_RXD[0]**	92	Input			Receive data
N2HET1[26]/**MII_RXD[1]**	92				
MIBSPI1NENA/N2HET1[23]/**MII_RXD[2]**	96		Pull Up	Fixed, 20uA	
MIBSPI5NENA/**MII_RXD[3]**	97				

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Table 2-14. PGE Ethernet Controller: Media Independent Interface (MII) (continued)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
N2HET1[10]/MII_TX_CLK/**MII_TX_AVCLK4**	118	I/O	Pull Down	-	MII output transmit clock
N2HET1[10]/**MII_TX_CLK**/MII_TX_AVCLK4	118				Transmit clock
MIBSPI5SOMI[0]/**MII_TXD[0]**	98	Output	Pull Up	-	Transmit data
MIBSPI5SIMO[0]/**MII_TXD[1]**	99				
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/**MII_TXD[2]**	105				
N2HET1[08]/MIBSPI1SIMO[1]/**MII_TXD[3]**	106		Pull Down	-	
MIBSPI5CLK/**MII_TXEN**	100		Pull Up	-	Transmit enable

2.4.1.11 System Module Interface

Table 2-15. PGE System Module Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
nPORRST	46	Input	Pull Down	100uA	Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of thespecified range. This terminal has a glitch filter. See Section 4.8.
nRST	116	I/O	Pull Up	100uA	System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pull-up resistor is connected to this terminal. This terminal has a glitch filter. See Section 4.8.
nERROR	117	I/O	Pull Down	20uA	ESM Error Signal Indicates error of high severity. See Section 4.18.

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2.4.1.12 Clock Inputs and Outputs

Table 2-16. PGE Clock Inputs and Outputs

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
OSCIN	18	Input	-	-	From external crystal/resonator, or external clock input
KELVIN_GND	19	Input			Kelvin ground for oscillator
OSCOUT	20	Output			To external crystal/resonator
ECLK	119	I/O	Pull Down	Programmable, 20uA	External prescaled clock output, or GIO.
GIOA[5]/**EXTCLKIN**	14	Input	Pull Down	20uA	External clock input #1

2.4.1.13 Test and Debug Modules Interface

Table 2-17. PGE Test and Debug Modules Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
TEST	34	I/O	Pull Down	Fixed, 100uA	Test enable
nTRST	109	Input			JTAG test hardware reset
RTCK	113	Output	-	-	JTAG return test clock
TCK	112	Input	Pull Down	Fixed, 100uA	JTAG test clock
TDI	110	I/O	Pull Up		JTAG test data in
TDO	111	I/O	Pull Down		JTAG test data out
TMS	108	I/O	Pull Up		JTAG test select

2.4.1.14 Flash Supply and Test Pads

Table 2-18. PGE Flash Supply and Test Pads

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
VCCP	134	Input	-	-	Flash pump supply
FLTP1	7				Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)].
FLTP2	8				

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2.4.1.15 Supply for Core Logic: 1.2V nominal

Table 2-19. PGE Supply for Core Logic: 1.2V nominal

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
VCC	17	-	-	-	Core supply
VCC	29				
VCC	45				
VCC	48				
VCC	49				
VCC	57				
VCC	87				
VCC	101				
VCC	114				
VCC	123				
VCC	137				
VCC	143				

2.4.1.16 Supply for I/O Cells: 3.3V nominal

Table 2-20. PGE Supply for I/O Cells: 3.3V nominal

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
VCCIO	10	Input	-	-	Operating supply for I/Os
VCCIO	26				
VCCIO	42				
VCCIO	104				
VCCIO	120				
VCCIO	136				

2.4.1.17 Ground Reference for All Supplies Except VCCAD

Table 2-21. PGE Ground Reference for All Supplies Except VCCAD

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	144 PGE				
VSS	11	Input	-	-	Ground reference
VSS	21				
VSS	27				
VSS	28				
VSS	43				
VSS	44				
VSS	47				
VSS	50				
VSS	56				
VSS	88				
VSS	102				
VSS	103				
VSS	115				
VSS	121				
VSS	122				
VSS	135				
VSS	138				

2.4.2 ZWT Package

2.4.2.1 Multi-Buffered Analog-to-Digital Converters (MibADC)

Table 2-22. ZWT Multi-Buffered Analog-to-Digital Converters (MibADC1, MibADC2)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
ADREFHI(1)	V15	Input	-	-	ADC high reference supply
ADREFLO(1)	V16	Input			ADC low reference supply
VCCAD(1)	W15	Power			Operating supply for ADC
VSSAD	V19	Ground	-	-	ADC supply power
	W16				
	W18				
	W19				
AD1EVT/MII_RX_ER	N19	Input	Pull Down	Programmable, 20uA	ADC1 event trigger input, or GIO
MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]	V10	I/O	Pull Up	Programmable, 20uA	ADC2 event trigger input, or GIO
AD1IN[0]	W14	Input	-	-	ADC1 analog input
AD1IN[01]	V17				
AD1IN[02]	V18				
AD1IN[03]	T17				
AD1IN[04]	U18				
AD1IN[05]	R17				
AD1IN[06]	T19				
AD1IN[07]	V14				
AD1IN[08] / AD2IN[08]	P18	Input	-	-	ADC1/ADC2 shared analog inputs
AD1IN[09] / AD2IN[09]	W17				
AD1IN[10] / AD2IN[10]	U17				
AD1IN[11] / AD2IN[11]	U19				
AD1IN[12] / AD2IN[12]	T16				
AD1IN[13] / AD2IN[13]	T18				
AD1IN[14] / AD2IN[14]	R18				
AD1IN[15] / AD2IN[15]	P19				
AD1IN[16] / AD2IN[0]	V13				
AD1IN[17] / AD2IN[01]	U13				
AD1IN[18] / AD2IN[02]	U14				
AD1IN[19] / AD2IN[03]	U16				
AD1IN[20] / AD2IN[04]	U15				
AD1IN[21] / AD2IN[05]	T15				
AD1IN[22] / AD2IN[06]	R19				
AD1IN[23] / AD2IN[07]	R16				

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.

2.4.2.2 Enhanced High-End Timer Modules (N2HET)

Table 2-23. ZWT Enhanced High-End Timer Modules (N2HET)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
N2HET1[0]/SPI4CLK	K18	I/O	Pull Down	Programmable, 20uA	N2HET1 time input capture or output compare, or GIO. Each terminal has a suppression filter that ignores input pulses smaller than a programmable duration.
N2HET1[01]/SPI4NENA/N2HET2[8]	V2				
N2HET1[02]/SPI4SIMO	W5				
N2HET1[03]/SPI4NCS[0]/N2HET2[10]	U1				
N2HET1[04]	B12				
N2HET1[05]/SPI4SOMI/N2HET2[12]	V6				
N2HET1[06]/SCIRX	W3				
N2HET1[07]/N2HET2[14]	T1				
N2HET1[08]/MIBSPI1SIMO[1]/MII_TXD[3]	E18				
N2HET1[09]/N2HET2[16]	V7				
N2HET1[10]/MII_TX_CLK/MII_TX_AVCLK4	D19				
N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]	E3				
N2HET1[12]/MII_CRS	B4				
N2HET1[13]/SCITX	N2				
N2HET1[14]	A11				
N2HET1[15]/MIBSPI1NCS[4]	N1				
N2HET1[16]	A4				
N2HET1[17]	A13				
N2HET1[18]	J1				
N2HET1[19]	B13				
N2HET1[20]	P2				
N2HET1[21]	H4				
N2HET1[22]	B3				
N2HET1[23]	J4				
N2HET1[24]/MIBSPI1NCS[5]/MII_RXD[0]	P1				
N2HET1[25]	M3				
N2HET1[26]/MII_RXD[1]	A14				
N2HET1[27]	A9				
N2HET1[28]/MII_RX_CLK/MII_RX_AVCLK4	K19				
N2HET1[29]	A3				
N2HET1[30]/MII_RX_DV	B11				
N2HET1[31]	J17				

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Table 2-23. ZWT Enhanced High-End Timer Modules (N2HET) (continued)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
GIOA[2]/**N2HET2[0]**	C1	I/O	Pull Down	Programmable, 20uA	N2HET2 time input capture or output compare, or GIO. Each terminal has a suppression filter that ignores input pulses smaller than a programmable duration.
EMIF_ADDR[0]/**N2HET2[1]**	D4				
GIOA[3]/**N2HET2[2]**	E1				
EMIF_ADDR[1]/**N2HET2[3]**	D5				
GIOA[6]/**N2HET2[4]**	H3				
EMIF_BA[1]/**N2HET2[5]**	D16				
GIOA[7]/**N2HET2[6]**	M1				
EMIF_nCS[0]/RTP_DATA[15]/**N2HET2[7]**	N17				
N2HET1[01]/SPI4NENA/**N2HET2[8]**	V2				
EMIF_nCS[3]/RTP_DATA[14]/**N2HET2[9]**	K17				
N2HET1[03]/SPI4NCS[0]/**N2HET2[10]**	U1				
EMIF_ADDR[6]/RTP_DATA[13]/**NHET2[11]**	C4				
N2HET1[05]/SPI4SOMI/**N2HET2[12]**	V6				
EMIF_ADDR[7]/RTP_DATA[12]/**NHET2[13]**	C5				
N2HET1[07]/**N2HET2[14]**	T1				
EMIF_ADDR[8]/RTP_DATA[11]/**N2HET2[15]**	C6				
N2HET1[09]/**N2HET2[16]**	V7				
N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]**	E3				

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2.4.2.3 General-Purpose Input / Output (GIO)

Table 2-24. ZWT General-Purpose Input / Output (GIO)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
GIOA[0]	A5	I/O	Pull Down	Programmable, 20uA	General-purpose I/O. All GIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges.
GIOA[1]	C2				
GIOA[2]/N2HET2[0]	C1				
GIOA[3]/N2HET2[2]	E1				
GIOA[4]	A6				
GIOA[5]/EXTCLKIN	B5				
GIOA[6]/N2HET2[4]	H3				
GIOA[7]/N2HET2[6]	M1				
GIOB[0]	M2				
GIOB[1]	K2				
GIOB[2]	F2				
GIOB[3]	W10				
GIOB[4]	G1				
GIOB[5]	G2				
GIOB[6]	J2				
GIOB[7]	F1				

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2.4.2.4 Controller Area Network Controllers (DCAN)

Table 2-25. ZWT Controller Area Network Controllers (DCAN)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
CAN1RX	B10	I/O	Pull Up	Programmable, 20uA	CAN1 receive, or GIO
CAN1TX	A10				CAN1 transmit, or GIO
CAN2RX	H1				CAN2 receive, or GIO
CAN2TX	H2				CAN2 transmit, or GIO
CAN3RX	M19				CAN3 receive, or GIO
CAN3TX	M18				CAN3 transmit, or GIO

2.4.2.5 Local Interconnect Network Interface Module (LIN)

Table 2-26. ZWT Local Interconnect Network Interface Module (LIN)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
LINRX	A7	I/O	Pull Up	Programmable, 20uA	LIN receive, or GIO
LINTX	B7				LIN transmit, or GIO

2.4.2.6 Standard Serial Communication Interface (SCI)

Table 2-27. ZWT Standard Serial Communication Interface (SCI)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
N2HET1[06]/**SCIRX**	W3	I/O	Pull Down	Programmable, 20uA	SCI receive, or GIO
N2HET1[13]/**SCITX**	N2				SCI transmit, or GIO

2.4.2.7 Inter-Integrated Circuit Interface Module (I2C)

Table 2-28. ZWT Inter-Integrated Circuit Interface Module (I2C)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27]	B2	I/O	Pull Up	Programmable, 20uA	I2C serial data, or GIO
MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29]	C3				I2C serial clock, or GIO

2.4.2.8 Standard Serial Peripheral Interface (SPI)

Table 2-29. ZWT Standard Serial Peripheral Interface (SPI)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
SPI2CLK	E2	I/O	Pull Up	Programmable, 20uA	SPI2 clock, or GIO
SPI2NCS[0]	N3				SPI2 chip select, or GIO
SPI2NENA/**SPI2NCS[1]**	D3				SPI2 chip select, or GIO
SPI2NENA/SPI2NCS[1]	D3				SPI2 enable, or GIO
SPI2SIMO	D1				SPI2 slave-input master-output, or GIO
SPI2SOMI	D2				SPI2 slave-output master-input, or GIO
N2HET1[0]/**SPI4CLK**	K18	I/O	Pull Down	Programmable, 20uA	SPI4 clock, or GIO
N2HET1[03]/**SPI4NCS[0]**/N2HET2[10]	U1				SPI4 chip select, or GIO
N2HET1[01]/**SPI4NENA**/N2HET2[8]	V2				SPI4 enable, or GIO
N2HET1[02]/**SPI4SIMO**	W5				SPI4 slave-input master-output, or GIO
N2HET1[05]/**SPI4SOMI**/N2HET2[12]	V6				SPI4 slave-output master-input, or GIO

2.4.2.9 Multi-Buffered Serial Peripheral Interface Modules (MibSPI)

Table 2-30. ZWT Multi-Buffered Serial Peripheral Interface Modules (MibSPI)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
MIBSPI1CLK	F18	I/O	Pull Up	Programmable, 20uA	MibSPI1 clock, or GIO
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/MII_TXD[2]	R2				MibSPI1 chip select, or GIO
MIBSPI1NCS[1]/N2HET1[17]/MII_COL	F3				
MIBSPI1NCS[2]/N2HET1[19]/MDIO	G3				
MIBSPI1NCS[3]/N2HET1[21]	J3				
N2HET1[15]/**MIBSPI1NCS[4]**	N1		Pull Down	Programmable, 20uA	MibSPI1 chip select, or GIO
N2HET1[24]/**MIBSPI1NCS[5]**/MII_RXD[0]	P1				
MIBSPI1NENA/N2HET1[23]/MII_RXD[2]	G19		Pull Up	Programmable, 20uA	MibSPI1 enable, or GIO
MIBSPI1SIMO	F19				MibSPI1 slave-in master-out, or GIO
N2HET1[08]/**MIBSPI1SIMO[1]**/MII_TXD[3]	E18		Pull Down	Programmable, 20uA	MibSPI1 slave-in master-out, or GIO
MIBSPI1SOMI	G18		Pull Up	Programmable, 20uA	MibSPI1 slave-out master-in, or GIO
MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/MII_TXD[2]	R2				
MIBSPI3CLK	V9	I/O	Pull Up	Programmable, 20uA	MibSPI3 clock, or GIO
MIBSPI3NCS[0]/AD2EVT/GIOB[2]	V10				MibSPI3 chip select, or GIO
MIBSPI3NCS[1]/N2HET1[25]/MDCLK	V5				
MIBSPI3NCS[2]/I2C_SDA/N2HET1[27]	B2				
MIBSPI3NCS[3]/I2C_SCL/N2HET1[29]	C3				
N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18]	E3		Pull Up	Programmable, 20uA	MibSPI3 chip select, or GIO
MIBSPI3NENA/**MIBSPI3NCS[5]**/N2HET1[31]	W9		Pull Up	Programmable, 20uA	MibSPI3 chip select, or GIO
MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]	W9				MibSPI3 enable, or GIO
MIBSPI3SIMO	W8				MibSPI3 slave-in master-out, or GIO
MIBSPI3SOMI	V8				MibSPI3 slave-out master-in, or GIO
MIBSPI5CLK/DMM_DATA[4]/MII_TXEN	H19	I/O	Pull Up	Programmable, 20uA	MibSPI5 clock, or GIO
MIBSPI5NCS[0]/DMM_DATA[5]	E19				MibSPI5 chip select, or GIO
MIBSPI5NCS[1]/DMM_DATA[6]	B6				
MIBSPI5NCS[2]/DMM_DATA[2]	W6				
MIBSPI5NCS[3]/DMM_DATA[3]	T12				
MIBSPI5NENA/DMM_DATA[7]/MII_RXD[3]	H18				MibSPI5 enable, or GIO
MIBSPI5SIMO[0]/DMM_DATA[8]/MII_TXD[1]	J19				MibSPI5 slave-in master-out, or GIO
MIBSPI5SIMO[1]/DMM_DATA[9]	E16				
MIBSPI5SIMO[2]/DMM_DATA[10]	H17				
MIBSPI5SIMO[3]/DMM_DATA[11]	G17				
MIBSPI5SOMI[0]/DMM_DATA[12]/MII_TXD[0]	J18				
MIBSPI5SOMI[1]/DMM_DATA[13]	E17				
MIBSPI5SOMI[2]/DMM_DATA[14]	H16				
MIBSPI5SOMI[3]/DMM_DATA[15]	G16				

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2.4.2.10 Ethernet Controller

Table 2-31. ZWT Ethernet Controller: MDIO Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
MIBSPI3NCS[1]/N2HET1[25]/**MDCLK**	V5	Output	Pull Up	-	Serial clock output
MIBSPI1NCS[2]/N2HET1[19]/**MDIO**	G3	I/O	Pull Up	Fixed, 20uA	Serial data input/output

2.4.2.11 External Memory Interface (EMIF)

Table 2-32. External Memory Interface (EMIF)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
EMIF_CKE	L3	Output	Pull Down	-	EMIF Clock Enablen
EMIF_CLK	K3	I/O			EMIF clock. This is an output signal in functional mode. It is gated off by default, so that the signal is tri-stated. PINMUX29[8] must be cleared to enable this output.
EMIF_nWE/**EMIF_RNW**	D17	Output	Pull Up	-	EMIF Read-Not-Write
ETMDATA[13]/**EMIF_nOE**	E12		Pull Down	-	EMIF Read Enable
EMIF_nWAIT	P3	I/O	Pull Up	Fixed, 20uA	EMIF Extended Wait Signal
EMIF_nWE/EMIF_RNW	D17	Output	Pull Up	-	EMIF Write Enable.
EMIF_nCAS	R4	Output			EMIF column address strobe
EMIF_nRAS	R3	Output			EMIF row address strobe
EMIF_nCS[0]/RTP_DATA[15]/N2HET2[7]	N17	Output			EMIF chip select, synchronous
EMIF_nCS[2]	L17	Output			EMIF chip selects, asynchronous This applies to chip selects 2, 3 and 4
EMIF_nCS[3]/RTP_DATA[14]/N2HET2[9]	K17	Output			
EMIF_nCS[4]/RTP_DATA[07]	M17	Output			

Table 2-32. External Memory Interface (EMIF) (continued)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
ETMDATA[15]/**EMIF_nDQM[0]**	E10	Output	Pull Down	-	EMIF Data Mask or Write Strobe. Data mask for SDRAM devices, write strobe for connected asynchronous devices.
ETMDATA[14]/**EMIF_nDQM[1]**	E11	Output			
ETMDATA[12]/**EMIF_BA[0]**	E13	Output			EMIF bank address or address line
EMIF_BA[1]/N2HET2[5]	D16	Output			EMIF bank address or address line
EMIF_ADDR[0]/N2HET2[1]	D4	Output			EMIF address
EMIF_ADDR[1]/N2HET2[3]	D5	Output			
ETMDATA[11]/**EMIF_ADDR[2]**	E6	Output			
ETMDATA[10]/**EMIF_ADDR[3]**	E7	Output			
ETMDATA[09]/**EMIF_ADDR[4**	E8	Output			
ETMDATA[08]/**EMIF_ADDR[5]**	E9	Output			
EMIF_ADDR[6]/RTP_DATA[13]	C4	Output			
EMIF_ADDR[7]/RTP_DATA[12]	C5	Output			
EMIF_ADDR[8]/RTP_DATA[11]	C6	Output			
EMIF_ADDR[9]/RTP_DATA[10]	C7	Output			
EMIF_ADDR[10]/RTP_DATA[09]	C8	Output			
EMIF_ADDR[11]/RTP_DATA[08]	C9	Output			
EMIF_ADDR[12]/RTP_DATA[06]	C10	Output			
EMIF_ADDR[13]/RTP_DATA[05]	C11	Output			
EMIF_ADDR[14]/RTP_DATA[04]	C12	Output			
EMIF_ADDR[15]/RTP_DATA[03]	C13	Output			
EMIF_ADDR[16]/RTP_DATA[02]	D14	Output			
EMIF_ADDR[17]/RTP_DATA[01]	C14	Output	Pull Down	-	
EMIF_ADDR[18]/RTP_DATA[0]	D15	Output			
EMIF_ADDR[19]/RTP_nENA	C15	Output			
EMIF_ADDR[20]/RTP_nSYNC	C16	Output			
EMIF_ADDR[21]/RTP_CLK	C17	Output			
ETMDATA[16]/**EMIF_DATA[0]**	K15	I/O	Pull Down	Fixed, 20uA	EMIF Data
ETMDATA[17]/**EMIF_DATA[1]**	L15	I/O			
ETMDATA[18]/**EMIF_DATA[2]**	M15	I/O			
ETMDATA[19]/**EMIF_DATA[3]**	N15	I/O			
ETMDATA[20]/**EMIF_DATA[4]**	E5	I/O			
ETMDATA[21]/**EMIF_DATA[5]**	F5	I/O			
ETMDATA[22]/**EMIF_DATA[6]**	G5	I/O			
ETMDATA[23]/**EMIF_DATA[7]**	K5	I/O			
ETMDATA[24]/**EMIF_DATA[8]**	L5	I/O			
ETMDATA[25]/**EMIF_DATA[9]**	M5	I/O			
ETMDATA[26]/**EMIF_DATA[10]**	N5	I/O			
ETMDATA[27]/**EMIF_DATA[11]**	P5	I/O			
ETMDATA[28]/**EMIF_DATA[12]**	R5	I/O			
ETMDATA[29]/**EMIF_DATA[13]**	R6	I/O			
ETMDATA[30]/**EMIF_DATA[14]**	R7	I/O			
ETMDATA[31]/**EMIF_DATA[15]**	R8	I/O			

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2.4.2.12 Embedded Trace Macrocell for Cortex-R4F CPU (ETM-R4F)

Table 2-33. Embedded Trace Macrocell for Cortex-R4F CPU (ETM-R4F)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
ETMTRACECLKIN/EXTCLKIN2	R9	Input	Pull Down	Fixed, 20uA	ETM Trace Clock Input
ETMTRACECLKOUT	R10	Output	Pull Down	-	ETM Trace Clock Output
ETMTRACECTL	R11	Output	Pull Down	-	ETM trace control
ETMDATA[0]	R12				ETM data
ETMDATA[01]	R13				
ETMDATA[02]	J15				
ETMDATA[03]	H15				
ETMDATA[04]	G15				
ETMDATA[05]	F15				
ETMDATA[06]	E15				
ETMDATA[07]	E14				
ETMDATA[08]/EMIF_ADDR[5]	E9				
ETMDATA[09]/EMIF_ADDR[4]	E8				
ETMDATA[10]/EMIF_ADDR[3]	E7				
ETMDATA[11]/EMIF_ADDR[2]	E6				
ETMDATA[12]/EMIF_BA[0]	E13				
ETMDATA[13]/EMIF_nOE	E12				
ETMDATA[14]/EMIF_nDQM[1]	E11				
ETMDATA[15]/EMIF_nDQM[0]	E10				
ETMDATA[16]/EMIF_DATA[0]	K15				
ETMDATA[17]/EMIF_DATA[1]	L15				
ETMDATA[18]/EMIF_DATA[2]	M15				
ETMDATA[19]/EMIF_DATA[3]	N15				
ETMDATA[20]/EMIF_DATA[4]	E5				
ETMDATA[21]/EMIF_DATA[5]	F5				
ETMDATA[22]/EMIF_DATA[6]	G5				
ETMDATA[23]/EMIF_DATA[7]	K5				
ETMDATA[24]/EMIF_DATA[8]	L5				
ETMDATA[25]/EMIF_DATA[9]	M5				
ETMDATA[26]/EMIF_DATA[10]	N5				
ETMDATA[27]/EMIF_DATA[11]	P5				
ETMDATA[28]/EMIF_DATA[12]	R5				
ETMDATA[29]/EMIF_DATA[13]	R6				
ETMDATA[30]/EMIF_DATA[14]	R7				
ETMDATA[31]/EMIF_DATA[15]	R8				

2.4.2.13 RAM Trace Port (RTP)

Table 2-34. RAM Trace Port (RTP)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
EMIF_ADDR[21]/**RTP_CLK**	C17	I/O	Pull Down	Programmable, 20uA	RTP packet clock, or GIO
EMIF_ADDR[19]/**RTP_nENA**	C15	I/O			RTP packet handshake, or GIO
EMIF_ADDR[20]/**RTP_nSYNC**	C16	I/O			RTP synchronization, or GIO
EMIF_ADDR[18]/**RTP_DATA[0]**	D15	I/O			RTP packet data, or GIO
EMIF_ADDR[17]/**RTP_DATA[01]**	C14				
EMIF_ADDR[16]/**RTP_DATA[02]**	D14				
EMIF_ADDR[15]/**RTP_DATA[03]**	C13				
EMIF_ADDR[14]/**RTP_DATA[04]**	C12				
EMIF_ADDR[13]/**RTP_DATA[05]**	C11				
EMIF_ADDR[12]/**RTP_DATA[06]**	C10				
EMIF_nCS[4]/**RTP_DATA[07]**	M17		Pull Up	Programmable, 20uA	
EMIF_ADDR[11]/**RTP_DATA[08]**	C9		Pull Down	Programmable, 20uA	
EMIF_ADDR[10]/**RTP_DATA[09]**	C8				
EMIF_ADDR[9]/**RTP_DATA[10]**	C7				
EMIF_ADDR[8]/**RTP_DATA[11]**	C6				
EMIF_ADDR[7]/**RTP_DATA[12]**	C5				
EMIF_ADDR[6]/**RTP_DATA[13]**	C4				
EMIF_nCS[0]/**RTP_DATA[15]**/N2HET2[7]	N17				
EMIF_nCS[3]/**RTP_DATA[14]**/N2HET2[9]	K17		Pull Up	Programmable, 20uA	

2.4.2.14 Data Modification Module (DMM)

Table 2-35. Data Modification Module (DMM)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
DMM_CLK	F17	I/O	Pull Up	Programmable, 20uA	DMM clock, or GIO
DMM_nENA	F16				DMM handshake, or GIO
DMM_SYNC	J16				DMM synchronization, or GIO
DMM_DATA[0]	L19				DMM data, or GIO
DMM_DATA[1]	L18				
MIBSPI5NCS[2]/**DMM_DATA[2]**	W6				
MIBSPI5NCS[3]/**DMM_DATA[3]**	T12				
MIBSPI5CLK/**DMM_DATA[4]**/MII_TXEN	H19				
MIBSPI5NCS[0]/**DMM_DATA[5]**	E19				
MIBSPI5NCS[1]/**DMM_DATA[6]**	B6				
MIBSPI5NENA/**DMM_DATA[7]**/MII_RXD[3]	H18				
MIBSPI5SIMO[0]/**DMM_DATA[8]**/MII_TXD[1]	J19				
MIBSPI5SIMO[1]/**DMM_DATA[9]**	E16				
MIBSPI5SIMO[2]/**DMM_DATA[10]**	H17				
MIBSPI5SIMO[3]/**DMM_DATA[11]**	G17				
MIBSPI5SOMI[0]/**DMM_DATA[12]**/MII_TXD[0]	J18				
MIBSPI5SOMI[1]/**DMM_DATA[13]**	E17				
MIBSPI5SOMI[2]/**DMM_DATA[14]**	H16				
MIBSPI5SOMI[3]/**DMM_DATA[15]**	G16				

2.4.2.15 System Module Interface

Table 2-36. ZWT System Module Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
nPORRST	W7	Input	Pull Down	100uA	Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of thespecified range. This terminal has a glitch filter. See Section 4.8.
nRST	B17	I/O	Pull Up	100uA	System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pull-up resistor is connected to this terminal. This terminal has a glitch filter. See Section 4.8.
nERROR	B14	I/O	Pull Down	20uA	ESM Error Signal Indicates error of high severity. See Section 4.18.

2.4.2.16 Clock Inputs and Outputs

Table 2-37. ZWT Clock Inputs and Outputs

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
OSCIN	K1	Input	-	-	From external crystal/resonator, or external clock input
KELVIN_GND	L2	Input			Kelvin ground for oscillator
OSCOUT	L1	Output			To external crystal/resonator
ECLK	A12	I/O	Pull Down	Programmable, 20uA	External prescaled clock output, or GIO.
GIOA[5]/**EXTCLKIN**	B5	Input	Pull Down	20uA	External clock input #1
ETMTRACECLKIN/**EXTCLKIN2**	R9	Input			External clock input #2
VCCPLL	P11	Input		-	Dedicated core supply for PLL's

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2.4.2.17 Test and Debug Modules Interface

Table 2-38. ZWT Test and Debug Modules Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
TEST	U2	I/O	Pull Down	Fixed, 100uA	Test enable
nTRST	D18	Input			JTAG test hardware reset
RTCK	A16	Output	-	-	JTAG return test clock
TCK	B18	Input	Pull Down	Fixed, 100uA	JTAG test clock
TDI	A17	I/O	Pull Up		JTAG test data in
TDO	C18	I/O	Pull Down		JTAG test data out
TMS	C19	I/O	Pull Up		JTAG test select

2.4.2.18 Flash Supply and Test Pads

Table 2-39. ZWT Flash Supply and Test Pads

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
VCCP	F8	Input	-	-	Flash pump supply
FLTP1	J5				Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)].
FLTP2	H5				

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2.4.2.19 No Connects

Table 2-40. No Connects

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
NC	D6	-	-	-	No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. Any other ball marked as "NC" may be internally connected to some functionality. It is recommended for such balls to be left unconnected.
NC	D7	-	-	-	
NC	D8	-	-	-	
NC	D9	-	-	-	
NC	D10	-	-	-	
NC	D11	-	-	-	
NC	D12	-	-	-	
NC	E4	-	-	-	
NC	F4	-	-	-	
NC	G4	-	-	-	
NC	K4	-	-	-	
NC	L4	-	-	-	
NC	M4	-	-	-	
NC	N4	-	-	-	
NC	N18	-	-	-	
NC	P4		-		
NC	P15	-	-	-	
NC	P16	-	-	-	
NC	P17	-	-	-	
NC	R1	-	-	-	
NC	R14	-	-	-	
NC	R15	-	-	-	
NC	T5	-	-	-	
NC	T6	-	-	-	
NC	T7	-	-	-	
NC	T8	-	-	-	
NC	T13	-	-	-	
NC	T14	-	-	-	
NC	V4	-	-	-	
NC	W4	-	-	-	

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2.4.2.20 Supply for Core Logic: 1.2V nominal

Table 2-41. ZWT Supply for Core Logic: 1.2V nominal

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
VCC	F9	-	-	-	Core supply
VCC	F10				
VCC	H10				
VCC	J14				
VCC	K6				
VCC	-				
VCC	K8				
VCC	K12				
VCC	K14				
VCC	L6				
VCC	M10				
VCC	P10				

2.4.2.21 Supply for I/O Cells: 3.3V nominal

Table 2-42. ZWT Supply for I/O Cells: 3.3V nominal

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
VCCIO	F6	Input	-	-	Operating supply for I/Os
VCCIO	F7				
VCCIO	F11				
VCCIO	F12				
VCCIO	F13				
VCCIO	F14				
VCCIO	G6				
VCCIO	G14				
VCCIO	H6				
VCCIO	H14				
VCCIO	J6				
VCCIO	L14				
VCCIO	M6				
VCCIO	M14				
VCCIO	N6				
VCCIO	N14				
VCCIO	P6				
VCCIO	P7				
VCCIO	P8				
VCCIO	P9				
VCCIO	P12				
VCCIO	P13				
VCCIO	P14				

2.4.2.22 Ground Reference for All Supplies Except VCCAD

Table 2-43. ZWT Ground Reference for All Supplies Except VCCAD

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 ZWT				
VSS	A1	Input	-	-	Ground reference
VSS	A2				
VSS	A18				
VSS	A19				
VSS	B1				
VSS	B19				
VSS	H8				
VSS	H9				
VSS	H11				
VSS	H12				
VSS	J8				
VSS	J9				
VSS	J10				
VSS	J11				
VSS	J12				
VSS	K9				
VSS	K10				
VSS	K11				
VSS	L8				
VSS	L9				
VSS	L10				
VSS	L11				
VSS	L12				
VSS	M8				
VSS	M9				
VSS	M11				
VSS	M12				
VSS	V1				
VSS	W1				
VSS	W2				

3 Device Operating Conditions

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range, (1)

Supply voltage range:	V_{CC} (2)	-0.3 V to 1.43 V
	V_{CCIO}, V_{CCP} (2)	-0.3 V to 4.1 V
	V_{CCAD}	-0.3 V to 5.5 V
Input voltage range:	All input pins	-0.3 V to 4.1 V
Input clamp current:	I_{IK} (V_I < 0 or V_I > V_{CCIO}) All pins, except AD1IN[23:0] and AD2IN[15:0]	±20 mA
	I_{IK} (V_I < 0 or V_I > V_{CCAD}) AD1IN[23:0] and AD2IN[15:0]	±10 mA
	Total	±40 mA
Operating free-air temperature range, T_A:		-40°C to 105°C
Operating junction temperature range, T_J:		-40°C to 125°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.

3.2 Device Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)	1.14	1.2	1.32	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.2	1.32	V
V_{CCIO}	Digital logic supply voltage (I/O)	3	3.3	3.6	V
V_{CCAD}	MibADC supply voltage	3	3.3	3.6	V
		4.5	5.0	5.25	
V_{CCP}	Flash pump supply voltage	3	3.3	3.6	V
V_{SS}	Digital logic supply ground		0		V
V_{SSAD}	MibADC supply ground	-0.1		0.1	V
$V_{ADREFHI}$	A-to-D high-voltage reference source	V_{SSAD}		V_{CCAD}	V
$V_{ADREFLO}$	A-to-D low-voltage reference source	V_{SSAD}		V_{CCAD}	V
T_A	Operating free-air temperature	-40		105	°C
T_J	Operating junction temperature	-40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}

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3.3 Switching Characteristics over Recommended Operating Conditions for Clock Domains

Table 3-1. Clock Domain Timing Specifications

Parameter	Description	Conditions		Min	Max	Unit
f_{HCLK}	HCLK - System clock frequency		Pipeline mode enabled		200	MHz
			Pipeline mode disabled		50	MHz
f_{GCLK}	GCLK - CPU clock frequency				f_{HCLK}	MHz
f_{VCLK}	VCLK - Primary peripheral clock frequency				100	MHz
f_{VCLK2}	VCLK2 - Secondary peripheral clock frequency				100	MHz
f_{VCLK3}	VCLK3 - Secondary peripheral clock frequency				100	MHz
f_{VCLKA1}	VCLKA1 - Primary asynchronous peripheral clock frequency				100	MHz
f_{VCLKA3}	VCLKA3 - Primary asynchronous peripheral clock frequency				48	
f_{VCLKA4}	VCLKA4 - Secondary asynchronous peripheral clock frequency				50	MHz
f_{RTICLK}	RTICLK - clock frequency				f_{VCLK}	MHz

3.4 Wait States Required

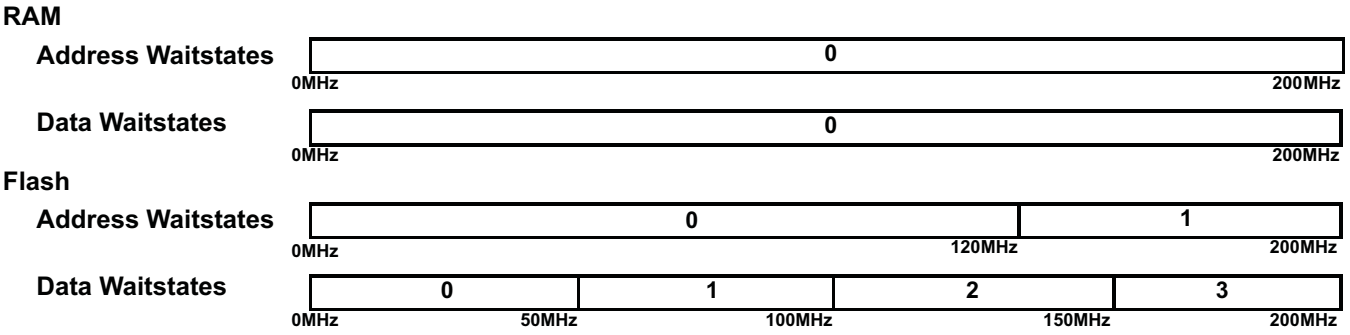

Figure 3-1. Wait States Scheme

As shown in the figure above, the TCM RAM can support program and data fetches at full CPU speed without any address or data wait states required.

The TCM flash can support zero address and data wait states up to a CPU speed of 50MHz in non-pipelined mode. The flash supports a maximum CPU clock speed of 200MHz in pipelined mode with one address wait state and three data wait states.

The flash wrapper defaults to non-pipelined mode with zero address wait state and one random-read data wait state.

3.5 Power Consumption Over Recommended Operating Conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} digital supply current (operating mode)		f_{HCLK} = 200MHz f_{VCLK} = 100MHz, Flash in pipelined mode, V_{CCmax}				mA
	V_{CC} Digital supply current (LBIST mode)		LBIST clock rate = 100MHz				mA
	VCC Digital supply current (PBIST mode)	Peak	PBIST ROM clock frequency = 100MHz			TBD	mA
		RMS					
I_{CCPLL}	VCCPLL digital supply current (operating mode)		V_{CCPLL} = $V_{CCPLLmax}$			10	mA
I_{CCIO}	V_{CCIO} Digital supply current (operating mode.		No DC load, V_{CCmax}			15	mA
I_{CCAD}	V_{CCAD} supply current (operating mode)		Single ADC operational, $V_{CCADmax}$			15	mA
			Both ADCs operational, $V_{CCADmax}$			30	
$I_{CCREFHI}$	AD_{REFHI} supply current (operating mode)		Single ADC operational, $AD_{REFHImax}$			5	mA
			Both ADCs operational, $AD_{REFHImax}$			10	
I_{CCP}	V_{CCP} pump supply current		read operation V_{CCPmax}			34	mA
			program, V_{CCPmax}			37	
			read from 1 bank and program another bank, V_{CCPmax}			55	
			erase, V_{CCPmax}			27	

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3.6 Input/Output Electrical Characteristics Over Recommended Operating Conditions(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis	All inputs		180			mV
V_{IL}	Low-level input voltage	All inputs(2)		-0.3		0.8	V
V_{IH}	High-level input voltage	All inputs(2)		2		V_{CCIO} + 0.3	V
V_{OL}	Low-level output voltage		I_{OL} = I_{OLmax}			0.2 V_{CCIO}	V
			I_{OL} = 50 µA, standard output mode			0.2	
			I_{OL} = 50 µA, low-EMI output mode (see Section 3.10)			0.2 V_{CCIO}	
V_{OH}	High-level output voltage		I_{OH} = I_{OHmax}	0.8 V_{CCIO}			V
			I_{OH} = 50 µA, standard output mode	V_{CCIO} -0.2			
			I_{OH} = 50 µA, low-EMI output mode (see Section 3.10)	0.8 V_{CCIO}			
I_{IC}	Input clamp current (I/O pins)		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIO} + 0.3	-2		2	mA
I_I	Input current (I/O pins)	I_{IH} Pulldown 20µA	V_I = V_{CCIO}	5		40	µA
		I_{IH} Pulldown 100µA	V_I = V_{CCIO}	40		195	
		I_{IL} Pullup 20µA	V_I = V_{SS}	-40		-5	
		I_{IL} Pullup 100µA	V_I = V_{SS}	-195		-40	
		All other pins	No pullup or pulldown	-1		1	
C_I	Input capacitance					2	pF
C_O	Output capacitance					3	pF

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the nPORRST pin.

3.7 Output Buffer Drive Strengths

Table 3-2. Output Buffer Drive Strengths

Low-level Output Current, I_{OL} for V_I=V_{OLmax} or High-level Output Current, I_{OH} for V_I=V_{OHmin}	Signals
8mA	MIBSPI5CLK, MIBSPI5SOMI[0], MIBSPI5SOMI[1], MIBSPI5SOMI[2], MIBSPI5SOMI[3], MIBSPI5SIMO[0], MIBSPI5SIMO[1], MIBSPI5SIMO[2], MIBSPI5SIMO[3], TMS, TDI, TDO, RTCK, SPI4CLK, SPI4SIMO, SPI4SOMI, nERROR, N2HET2[1], N2HET2[3], All EMIF Outputs and I/Os, All ETM Outputs
4mA	TEST, MIBSPI3SOMI, MIBSPI3SIMO, MIBSPI3CLK, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI1CLK, nRST

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Table 3-2. Output Buffer Drive Strengths (continued)

Low-level Output Current, I_{OL} for $V_I=V_{OLmax}$ or High-level Output Current, I_{OH} for $V_I=V_{OHmin}$	Signals
2mA zero-dominant	AD1EVT, CAN1RX, CAN1TX, CAN2RX, CAN2TX, CAN3RX, CAN3TX, DMM_CLK, DMM_DATA[0], DMM_DATA[1], DMM_nENA, DMM_SYNC, GIOA[0-7], GIOB[0-7], LINRX, LINTX, MIBSPI1NCS[0], MIBSPI1NCS[1-3], MIBSPI1NENA, MIBSPI3NCS[0-3], MIBSPI3NENA, MIBSPI5NCS[0-3], MIBSPI5NENA, N2HET1[0-31], N2HET2[0], N2HET2[2], N2HET2[4], N2HET2[5], N2HET2[6], N2HET2[7], N2HET2[8], N2HET2[9], N2HET2[10], N2HET2[11], N2HET2[12], N2HET2[13], N2HET2[14], N2HET2[15], N2HET2[16], N2HET2[18], SPI2NCS[0], SPI2NENA, SPI4NCS[0], SPI4NENA
selectable 8mA / 2mA	ECLK, SPI2CLK, SPI2SIMO, SPI2SOMI The default output buffer drive strength is 8mA for these signals.

3.8 Input Timings

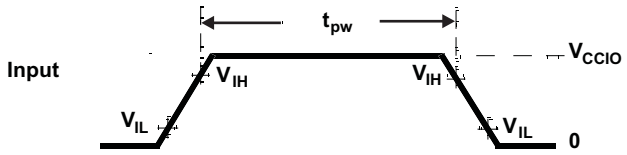

Figure 3-2. TTL-Level Inputs

Table 3-3. Timing Requirements for Inputs (1)

Parameter		MIN	MAX	Unit
t_{pw}	Input minimum pulse width	$t_{c(VCLK)}$ + 10 (2)		ns

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$
(2) The timing shown above is only valid for pin used in GIO mode.

3.9 Output Timings

Table 3-4. Switching Characteristics for Output Timings versus Load Capacitance (CL)

Parameter			MIN	MAX	Unit
Rise time, t_r	8mA low EMI pins (see Table 3-2)	CL = 15 pF		2.5	ns
		CL = 50 pF		4	
		CL = 100 pF		7.2	
		CL = 150 pF		12.5	
Fall time, t_f		CL = 15 pF		2.5	ns
		CL = 50 pF		4	
		CL = 100 pF		7.2	
		CL = 150 pF		12.5	

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Table 3-4. Switching Characteristics for Output Timings versus Load Capacitance (CL) (continued)

Parameter				MIN	MAX	Unit
Rise time, t_r	4mA low EMI pins (see Table 3-2)		CL = 15 pF		5.6	ns
			CL = 50 pF		10.4	
			CL = 100 pF		16.8	
			CL = 150 pF		23.2	
Fall time, t_f			CL = 15 pF		5.6	ns
			CL= 50 pF		10.4	
			CL = 100 pF		16.8	
			CL = 150 pF		23.2	
Rise time, t_r	2mA-z low EMI pins (see Table 3-2)		CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Rise time, t_r	Selectable 8mA / 2mA-z pins (see Table 3-2)	8mA mode	CL = 15 pF		2	ns
			CL = 50 pF		4	
			CL = 100 pF		8	
			CL = 150 pF		11	
Fall time, t_f			CL = 15 pF		2	ns
			CL = 50 pF		4	
			CL = 100 pF		8	
			CL = 150 pF		11	
Rise time, t_r		2mA-z mode	CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	

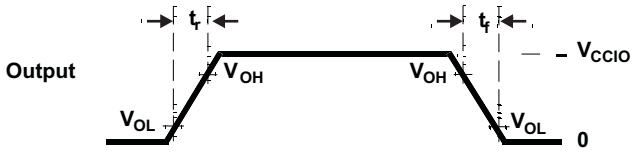

Figure 3-3. CMOS-Level Outputs

Table 3-5. Timing Requirements for Outputs(1)

Parameter		MIN	MAX	UNIT
$t_{d(parallel\_out)}$	Delay between low to high, or high to low transition of general-purpose output signals that can be configured by an application in parallel, e.g. all signals in a GIOA port, or all N2HET1 signals, etc.		5	ns

(1) This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check Table 3-2 for output buffer drive strength information on each signal.

3.10 Low-EMI Output Buffers

The low-EMI output buffer has been designed explicitly to address the issue of decoupling sources of emissions from the pins which they drive. This is accomplished by adaptively controlling the impedance of the output buffer, and is particularly effective with capacitive loads.

This is not the default mode of operation of the low-EMI output buffers and must be enabled by setting the system module GPCR1 register for the desired module or signal, as shown in . The adaptive impedance control circuit monitors the DC bias point of the output signal. The buffer internally generates two reference levels, VREFLOW and VREFHIGH, which are set to approximately 10% and 90% of VCCIO, respectively.

Once the output buffer has driven the output to a low level, if the output voltage is below VREFLOW, then the output buffer's impedance will increase to hi-Z. A high degree of decoupling between the internal ground bus and the output pin will occur with capacitive loads, or any load in which no current is flowing, e.g. the buffer is driving low on a resistive path to ground. Current loads on the buffer which attempt to pull the output voltage above VREFLOW will be opposed by the buffer's output impedance so as to maintain the output voltage at or below VREFLOW.

Conversely, once the output buffer has driven the output to a high level, if the output voltage is above VREFHIGH then the output buffer's impedance will again increase to hi-Z. A high degree of decoupling between internal power bus ad output pin will occur with capacitive loads or any loads in which no current is flowing, e.g. buffer is driving high on a resistive path to VCCIO. Current loads on the buffer which attempt to pull the output voltage below VREFHIGH will be opposed by the buffer's output impedance so as to maintain the output voltage at or above VREFHIGH.

The bandwidth of the control circuitry is relatively low, so that the output buffer in adaptive impedance control mode cannot respond to high-frequency noise coupling into the buffer's power buses. In this manner, internal bus noise approaching 20% peak-to-peak of VCCIO can be rejected.

Unlike standard output buffers which clamp to the rails, an output buffer in impedance control mode will allow a positive current load to pull the output voltage up to VCCIO + 0.6V without opposition. Also, a negative current load will pull the output voltage down to VSSIO – 0.6V without opposition. This is not an issue since the actual clamp current capability is always greater than the IOH / IOL specifications.

The low-EMI output buffers are automatically configured to be in the standard buffer mode when the device enters a low-power mode.

Table 3-6. Low-EMI Output Buffer Hookup

Module or Signal Name	Control Register to Enable Low-EMI Mode
Module: MibSPI1	GPREG1.0
Module: SPI2	GPREG1.1
Module: MibSPI3	GPREG1.2
Reserved	GPREG1.3
Signal: TMS	GPREG1.8
Signal: TDI	GPREG1.9
Signal: TDO	GPREG1.10
Signal: RTCK	GPREG1.11
Signal: TEST	GPREG1.12
Signal: nERROR	GPREG1.13
Reserved	GPREG1.14

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4 System Information and Electrical Specifications

4.1 Device Power Domains

The device core logic is split up into multiple power domains in order to optimize the power for a given application use case. There are 8 core power domains in total: PD1, PD2, PD3, PD4, PD5, RAM_PD1, RAM_PD2 and RAM_PD3.

The actual contents of these power domains are indicated in .

PD1 is an "always-ON" power domain, which cannot be turned off. Each of the other core power domains can be turned ON/OFF one time during device initialization as per the application requirement. Refer to the Power Management Module (PMM) chapter of the device technical reference manual for more details.

NOTE

The clocks to a module must be turned off before powering down the core domain that contains the module.

NOTE

The logic in the modules that are powered down loses its power completely. Any access to modules that are powered down results in an abort being generated. When power is restored, the modules power-up to their default states (after normal power-up). No register or memory contents are preserved in the core domains that are turned off.

4.2 Voltage Monitor Characteristics

A voltage monitor is implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies.

4.2.1 Important Considerations

- The voltage monitor does not eliminate the need of a voltage supervisor circuit to guarantee that the device is held in reset when the voltage supplies are out of range.
- The voltage monitor only monitors the core supply (VCC) and the I/O supply (VCCIO). The other supplies are not monitored by the VMON. For example, if the VCCAD or VCCP are supplied from a source different from that for VCCIO, then there is no internal voltage monitor for the VCCAD and VCCP supplies.

4.2.2 Voltage Monitor Operation

The voltage monitor generates the Power Good MCU signal (PGMCU) as well as the I/Os Power Good IO signal (PGIO) on the device. During power-up or power-down, the PGMCU and PGIO are driven low when the core or I/O supplies are lower than the specified minimum monitoring thresholds. The PGIO and PGMCU being low isolates the core logic as well as the I/O controls during the power-up or power-down of the supplies. This allows the core and I/O supplies to be powered up or down in any order.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a power-on reset. When the voltage monitor detects an out-of-range voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a power-on reset. The voltage monitor is disabled when the device enters a low power mode.

The VMON also incorporates a glitch filter for the nPORRST input. Refer to Section 4.3.3.1 for the timing information on this glitch filter.

Table 4-1. Voltage Monitoring Specifications

PARAMETER			MIN	TYP	MAX	UNIT
V_{MON}	Voltage monitoring thresholds	VCC low - VCC level below this threshold is detected as too low.	0.8	0.9	1.0	V
		VCC high - VCC level above this threshold is detected as too high.	1.40	1.7	2.1	
		VCCIO low - VCCIO level below this threshold is detected as too low.	1.9	2.4	2.9	

4.2.3 Supply Filtering

The VMON has the capability to filter glitches on the VCC and VCCIO supplies.

The following table shows the characteristics of the supply filtering. Glitches in the supply larger than the maximum specification cannot be filtered.

Table 4-2. VMON Supply Glitch Filtering Capability

Parameter	MIN	MAX
Width of glitch on VCC that can be filtered	250ns	1us
Width of glitch on VCCIO that can be filtered	250ns	1us

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4.3 Power Sequencing and Power On Reset

4.3.1 Power-Up Sequence

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage. The power-up sequence starts with the I/O voltage rising above the minimum I/O supply threshold, (see Table 4-4 for more details), core voltage rising above the minimum core supply threshold and the release of power-on reset. The high frequency oscillator will start up first and its amplitude will grow to an acceptable level. The oscillator start up time is dependent on the type of oscillator and is provided by the oscillator vendor. The different supplies to the device can be powered up in any order.

The device goes through the following sequential phases during power up.

Table 4-3. Power-Up Phases

Oscillator start-up and validity check	1032 oscillator cycles
eFuse autoload	1180 oscillator cycles
Flash pump power-up	688 oscillator cycles
Flash bank power-up	617 oscillator cycles
Total	**3517 oscillator cycles**

The CPU reset is released at the end of the above sequence and fetches the first instruction from address 0x00000000.

4.3.2 Power-Down Sequence

The different supplies to the device can be powered down in any order.

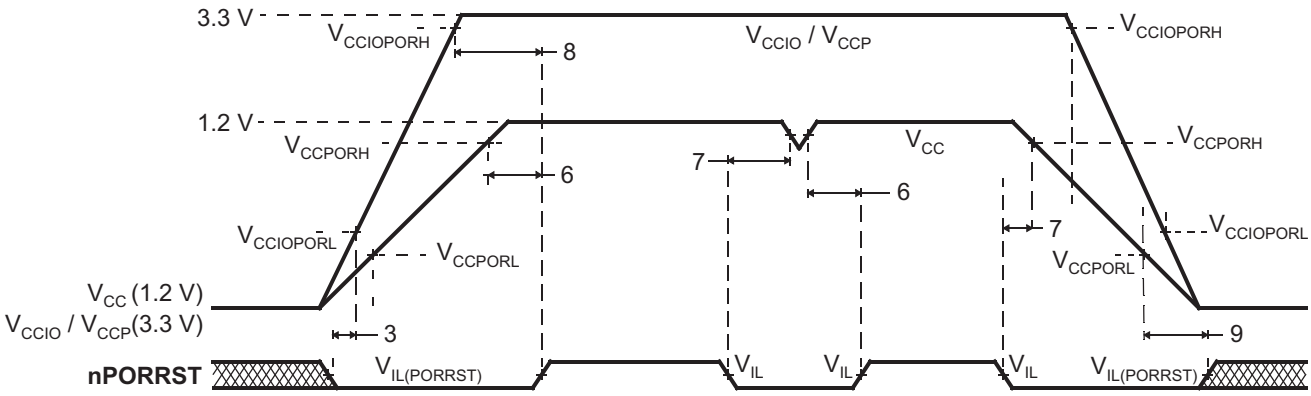
4.3.3 Power-On Reset: nPORRST

This is the power-on reset. This reset must be asserted by an external circuitry whenever the I/O or core supplies are outside the specified recommended range. This signal has a glitch filter on it. It also has an internal pulldown.

4.3.3.1 nPORRST Electrical and Timing Requirements

Table 4-4. Electrical Requirements for nPORRST

NO	Parameter		MIN	MAX	Unit
	V_{CCPORL}	V_{CC} low supply level when nPORRST must be active during power-up		0.5	V
	V_{CCPORH}	V_{CC} high supply level when nPORRST must remain active during power-up and become active during power down	1.14		V
	$V_{CCIOPORL}$	V_{CCIO} / V_{CCP} low supply level when nPORRST must be active during power-up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} / V_{CCP} high supply level when nPORRST must remain active during power-up and become active during power down	3.0		V
	$V_{IL(PORRST)}$	Low-level input voltage of nPORRST V_{CCIO} > 2.5V		0.2 * V_{CCIO}	V
		Low-level input voltage of nPORRST V_{CCIO} < 2.5V		0.5	V
3	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CCIO} and V_{CCP} > $V_{CCIOPORL}$ during power-up	0		ms
6	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} > V_{CCPORH}	1		ms
7	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CC} < V_{CCPORH} during power down	2		µs
8	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CCIO} and V_{CCP} > $V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} < V_{CCPORL}	0		ms
	$t_{f(nPORRST)}$	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset.	500	2000	ns



NOTE: There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage; this is just an exemplary drawing.

Figure 4-1. nPORRST Timing Diagram

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4.4 Warm Reset (nRST)

This is a bidirectional reset signal. The internal circuitry drives the signal low on detecting any device reset condition. An external circuit can assert a device reset by forcing the signal low. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.

This terminal has a glitch filter. It also has an internal pullup

4.4.1 Causes of Warm Reset

Table 4-5. Causes of Warm Reset

DEVICE EVENT	SYSTEM STATUS FLAG
Power-Up Reset	Exception Status Register, bit 15
Oscillator fail	Global Status Register, bit 0
PLL slip	Global Status Register, bits 8 and 9
Watchdog exception / Debugger reset	Exception Status Register, bit 13
CPU Reset (driven by the CPU STC)	Exception Status Register, bit 5
Software Reset	Exception Status Register, bit 4
External Reset	Exception Status Register, bit 3

4.4.2 nRST Timing Requirements

Table 4-6. nRST Timing Requirements(1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, nRST active after nPORRST inactive	1180 $t_{c(OSC)}$ + 1048$t_{c(OSC)}$		ns
	Valid time, nRST active (all other System reset conditions)	8$t_{c(VCLK)}$		
$t_{f(nRST)}$	Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	500	2000	ns

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see the switching characteristics for output timings versus load capacitance table.

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4.5 ARM© Cortex-R4F™ CPU Information

4.5.1 Summary of ARM Cortex-R4F™ CPU Features

The features of the ARM Cortex-R4F™ CPU include:

- An integer unit with integral EmbeddedICE-RT logic.
- High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced eXtensible Interfaces (AXI) for Level two (L2) master and slave interfaces.
- Floating Point Coprocessor
- Dynamic branch prediction with a global history buffer, and a 4-entry return stack
- Low interrupt latency.
- Non-maskable interrupt.
- A Harvard Level one (L1) memory system with:
  - Tightly-Coupled Memory (TCM) interfaces with support for error correction or parity checking memories
  - ARMv7-R architecture Memory Protection Unit (MPU) with 12 regions
- Dual core logic for fault detection in safety-critical applications.
- An L2 memory interface:
  - Single 64-bit master AXI interface
  - 64-bit slave AXI interface to TCM RAM blocks
- A debug interface to a CoreSight Debug Access Port (DAP).
- A trace interface to a CoreSight ETM-R4.
- A Performance Monitoring Unit (PMU).
- A Vectored Interrupt Controller (VIC) port.

For more information on the ARM Cortex-R4F™ CPU please see www.arm.com.

4.5.2 ARM Cortex-R4F™ CPU Features Enabled by Software

The following CPU features are disabled on reset and must be enabled by the application if required.

- ECC On Tightly-Coupled Memory (TCM) Accesses
- Harware Vectored Interrupt (VIC) Port
- Floating Point Coprocessor
- Memory Protection Unit (MPU)

4.5.3 Dual Core Implementation

The device has two Cortex-R4F cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed by 2 clock cycles as shown in Figure 4-3.

The CPUs have a diverse CPU placement given by following requirements:

- different orientation; e.g. CPU1 = "north" orientation, CPU2 = "flip west" orientation
- dedicated guard ring for each CPU

Figure 4-2. Dual - CPU Orientation

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4.5.4 Duplicate clock tree after GCLK

The CPU clock domain is split into two clock trees, one for each CPU, with the clock of the 2nd CPU running at the same frequency and in phase to the clock of CPU1. See Figure 4-3.

4.5.5 ARM Cortex-R4F™ CPU Compare Module (CCM) for Safety

This device has two ARM Cortex-R4F™ CPU cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in the figure below.

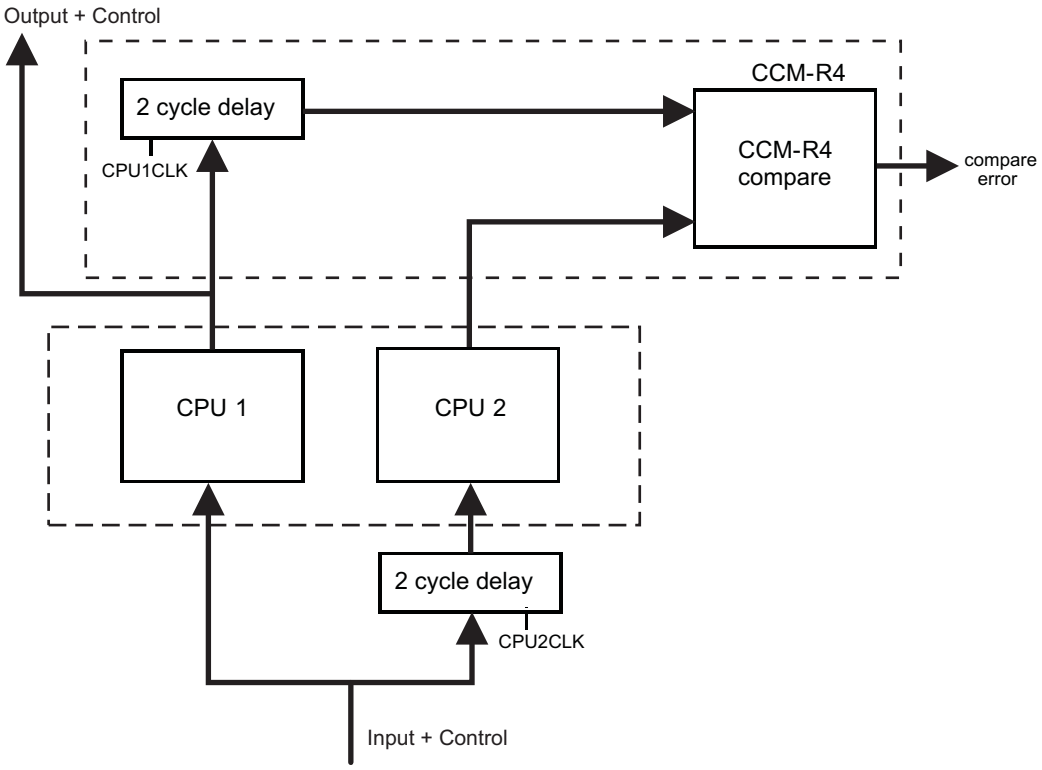


Figure 4-3. Dual Core Implementation

To avoid an erroneous CCM-R4 compare error, the application software must initialize the registers of both CPUs before the registers are used, including function calls where the register values are pushed onto the stack.

4.5.6 CPU Self-Test

The CPU STC (Self-Test Controller) is used to test the two Cortex-R4F CPU Cores using the Deterministic Logic BIST Controller as the test engine.

The main features of the self-test controller are:

- Ability to divide the complete test run into independent test intervals
- Capable of running the complete test as well as running few intervals at a time
- Ability to continue from the last executed interval (test set) as well as ability to restart from the beginning (First test set)
- Complete isolation of the self-tested CPU core from rest of the system during the self-test run
- Ability to capture the Failure interval number
- Timeout counter for the CPU self-test run as a fail-safe feature

4.5.6.1 Application Sequence for CPU Self-Test

1. Configure clock domain frequencies.
2. Select number of test intervals to be run.
3. Configure the timeout period for the self-test run.
4. Enable self-test.
5. Wait for CPU reset.
6. In the reset handler, read CPU self-test status to identify any failures.
7. Retrieve CPU state if required.

For more information see the RM48x Technical Reference Manual (SPNU481).

4.5.6.2 CPU Self-Test Clock Configuration

The maximum clock rate for the self-test is 100MHz. The STCCLK is divided down from the CPU clock. This divider is configured by the STCCLKDIV register at address 0xFFFFE108.

For more information see the RM48x Technical Reference Manual (SPNU481).

4.5.6.3 CPU Self-Test Coverage

Table 4-7 shows CPU test coverage achieved for each self-test interval. It also lists the cumulative test cycles. The test time can be calculated by multiplying the number of test cycles with the STC clock period.

Table 4-7. CPU Self-Test Coverage

INTERVALS	TEST COVERAGE, %	TEST CYCLES
0	0	0
1	62.13	1365
2	70.09	2730
3	74.49	4095
4	77.28	5460
5	79.28	6825
6	80.90	8190
7	82.02	9555
8	83.10	10920
9	84.08	12285
10	84.87	13650
11	85.59	15015
12	86.11	16380
13	86.67	17745
14	87.16	19110
15	87.61	20475
16	87.98	21840
17	88.38	23205
18	88.69	24570
19	88.98	25935
20	89.28	27300
21	89.50	28665
22	89.76	30030
23	90.01	31395
24	90.21	32760

4.6 Clocks

4.6.1 Clock Sources

The table below lists the available clock sources on the device. Each of the clock sources can be enabled or disabled using the CSDISx registers in the system module. The clock source number in the table corresponds to the control bit in the CSDISx register for that clock source.

The table also shows the default state of each clock source.

Table 4-8. Available Clock Sources

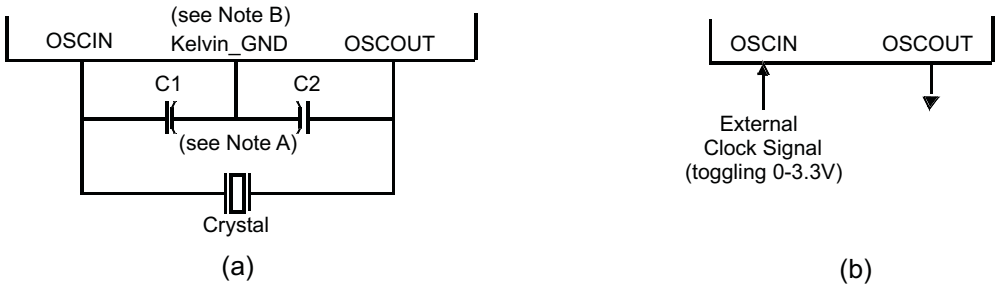
Clock Source #	Name	Description	Default State
0	OSCIN	Main Oscillator	Enabled
1	PLL1	Output From PLL1	Disabled
2	Reserved	Reserved	Disabled
3	EXTCLKIN1	External Clock Input #1	Disabled
4	CLK80K	Low Frequency Output of Internal Reference Oscillator	Enabled
5	CLK10M	High Frequency Output of Internal Reference Oscillator	Enabled
6	PLL2	Output From PLL2	Disabled
7	EXTCLKIN2	External Clock Input #2	Disabled

4.6.1.1 Main Oscillator

The oscillator is enabled by connecting the appropriate fundamental resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 4-4. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and low power modes.

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 3.3V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in the figure below.



Note A: The values of C1 and C2 should be provided by the resonator/crystal vendor.
Note B: Kelvin_GND should not be connected to any other GND.

Figure 4-4. Recommended Crystal/Clock Connection

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4.6.1.1.1 Timing Requirements for Main Oscillator

Table 4-9. Timing Requirements for Main Oscillator

Parameter		MIN	Type	MAX	Unit
tc(OSC)	Cycle time, OSCIN (when using a sine-wave input)	50		200	ns
tc(OSC_SQR)	Cycle time, OSCIN, (when input to the OSCIN is a square wave)	12.5		200	ns
tw(OSCIL)	Pulse duration, OSCIN low (when input to the OSCIN is a square wave)	6			ns
tw(OSCIH)	Pulse duration, OSCIN high (when input to the OSCIN is a square wave)	6			ns

4.6.1.2 Low Power Oscillator

The Low Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

4.6.1.2.1 Features

The main features of the LPO are:

- Supplies a clock at extremely low power for power-saving modes. This is connected as clock source # 4 of the Global Clock Module.
- Supplies a high-frequency clock for non-timing-critical systems. This is connected as clock source # 5 of the Global Clock Module.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

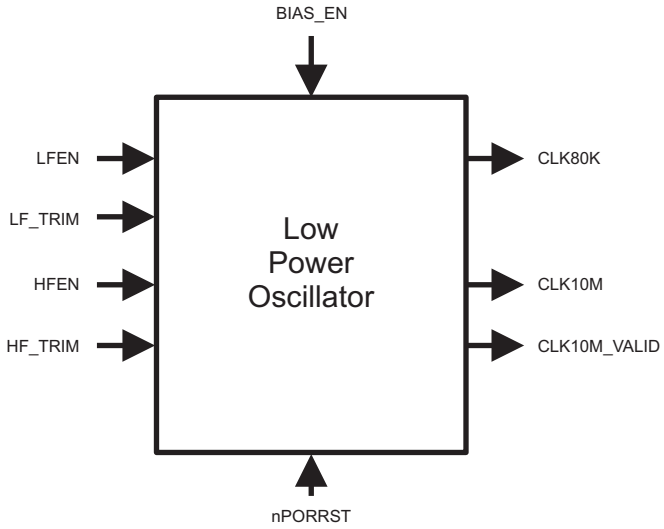

Figure 4-5. LPO Block Diagram

Figure 4-5 shows a block diagram of the internal reference oscillator. This is a low power oscillator (LPO) and provides two clock sources: one nominally 80KHz and one nominally 10MHz.

4.6.1.2.2 LPO Electrical and Timing Specifications

Table 4-10. LPO Specifications

Parameter		MIN	Type	MAX	Unit
LPO - HF oscillator	untrimmed frequency	5.5	9.6	19.5	MHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900µs)			10	µs
	cold startup time			900	µs
LPO - LF oscillator	untrimmed frequency	36	85	180	kHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900µs)			100	µs
	cold startup time			2000	µs

4.6.1.3 Phase Locked Loop (PLL) Clock Modules

The PLL is used to multiply the input frequency to some higher frequency.

The main features of the PLL are:

- Frequency modulation can be optionally superimposed on the synthesized frequency of PLL1. The frequency modulation capability of PLL2 is permanently disabled.
- Configurable frequency multipliers and dividers.
- Built-in PLL Slip monitoring circuit.
- Option to reset the device on a PLL slip detection.

4.6.1.3.1 Block Diagram

Figure 4-6 shows a high-level block diagram of the two PLL macros on this microcontroller. PLLCTL1 and PLLCTL2 are used to configure the multiplier and dividers for the PLL1. PLLCTL3 is used to configure the multiplier and dividers for PLL2.

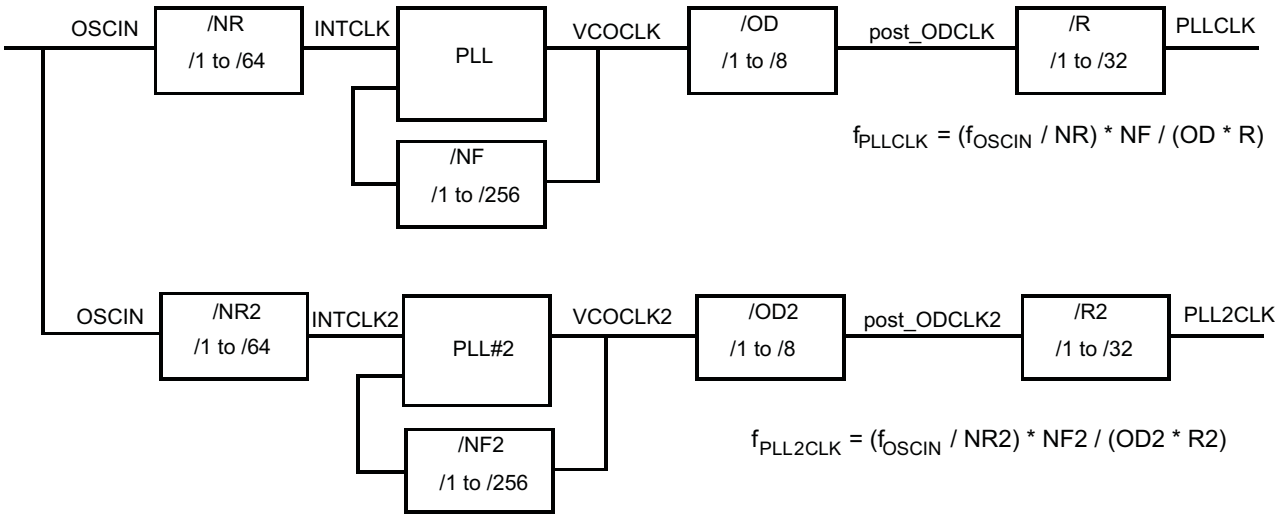

Figure 4-6. ZWT PLLx Block Diagram

4.6.1.3.2 PLL Timing Specifications

Table 4-11. PLL Timing Specifications

PARAMETER		MIN	MAX	UNIT
f_{INTCLK}	PLL1 Reference Clock frequency	1	$f_{(OSC\_SQR)}$	MHz
f_{post_ODCLK}	Post-ODCLK – PLL1 Post-divider input clock frequency		400	MHz
f_{VCOCLK}	VCOCLK – PLL1 Output Divider (OD) input clock frequency		550	MHz
$f_{INTCLK2}$	PLL2 Reference Clock frequency	1	$f_{(OSC\_SQR)}$	MHz
f_{post_ODCLK2}	Post-ODCLK – PLL2 Post-divider input clock frequency		400	MHz
$f_{VCOCLK2}$	VCOCLK – PLL2 Output Divider (OD) input clock frequency		550	MHz

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4.6.1.4 External Clock Inputs

The device supports up to two external clock inputs. This clock input must be a square wave input. The electrical and timing requirements for these clock inputs are specified below.

Table 4-12. External Clock Timing and Electrical Specifications

Parameter	Description	Min	Max	Unit
$f_{EXTCLKx}$	External clock input frequency		80	MHz
$t_{w(EXTCLKIN)H}$	EXTCLK high-pulse duration	6		ns
$t_{w(EXTCLKIN)L}$	EXTCLK low-pulse duration	6		ns
$v_{iL(EXTCLKIN)}$	Low-level input voltage	-0.3	0.8	V
$v_{iH(EXTCLKIN)}$	High-level input voltage	2	VCCIO + 0.3	V

4.6.2 Clock Domains

4.6.2.1 Clock Domain Descriptions

The table below lists the device clock domains and their default clock sources. The table also shows the system module control register that is used to select an available clock source for each clock domain.

Table 4-13. Clock Domain Descriptions

Clock Domain Name	Default Clock Source	Clock Source Selection Register	Description
HCLK	OSCIN	GHVSRC	• Is disabled via the CDDISx registers bit 1 • Used for all system modules including DMA, ESM
GCLK	OSCIN	GHVSRC	• Always the same frequency as HCLK • In phase with HCLK • Is disabled separately from HCLK via the CDDISx registers bit 0 • Can be divided by 1up to 8 when running CPU self-test (LBIST) using the CLKDIV field of the STCCLKDIV register at address 0xFFFFE108
GCLK2	OSCIN	GHVSRC	• Always the same frequency as GCLK • 2 cycles delayed from GCLK • Is disabled along with GCLK • Gets divided by the same divider setting as that for GCLK when running CPU self-test (LBIST)
VCLK	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Is disabled separately from HCLK via the CDDISx registers bit 2
VCLK2	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Frequency must be an integer multiple of VCLK frequency • Is disabled separately from HCLK via the CDDISx registers bit 3
VCLK3	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Is disabled separately from HCLK via the CDDISx registers bit 8
VCLKA1	VCLK	VCLKASRC	• Defaults to VCLK as the source • Is disabled via the CDDISx registers bit 4
VCLKA2	VCLK	VCLKASRC	• Defaults to VCLK as the source • Is disabled via the CDDISx registers bit 5
VCLKA3_S	VCLK	VCLKACON	• Defaults to VCLK as the source • Frequency can be as fast as HCLK frequency. • Is disabled via the CDDISx registers bit 10

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Table 4-13. Clock Domain Descriptions (continued)

Clock Domain Name	Default Clock Source	Clock Source Selection Register	Description
VCLKA3_DIVR	VCLK	VCLKACON1	• Divided down from the AVCLK3_S using the VCLKA3R field of the VCLKACON1 register at address 0xFFFFE140 • Frequency can be VCLKA3_S/1, VCLKA3_S/2, ..., or VCLKA3_S/8 • Default frequency is VCLKA3_S/2 • Is disabled separately via the VCLKACON1 register VCLKA3_DIV_CDDIS bit only if the VCLKA3_S clock is not disabled
VCLKA4	VCLK	VCLKACON1	• Defaults to VCLK as the source • Is disabled via the CDDISx registers bit 11
RTICLK	VCLK	RCLKSRC	• Defaults to VCLK as the source • If a clock source other than VCLK is selected for RTICLK, then the RTICLK frequency must be less than or equal to VCLK/3 – Application can ensure this by programming the RTI1DIV field of the RCLKSRC register, if necessary • Is disabled via the CDDISx registers bit 6

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4.6.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in the figures below.

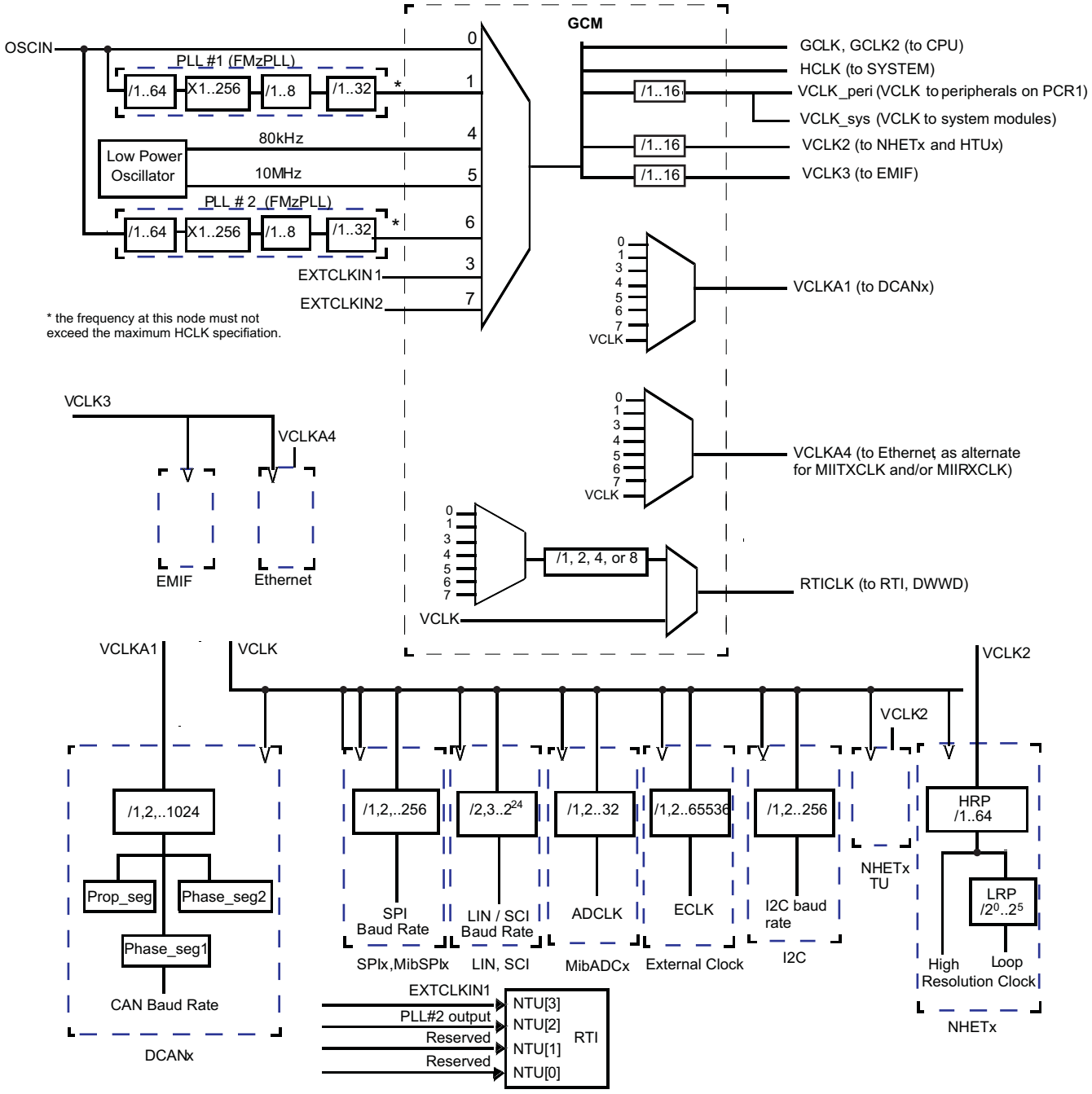

Figure 4-7. Device Clock Domains

4.6.3 Clock Test Mode

The RM4x platform architecture defines a special mode that allows various clock signals to be brought out on to the ECLK pin and N2HET1[12] device outputs. This mode is called the Clock Test mode. It is very useful for debugging purposes and can be configured via the CLKTEST register in the system module.

Table 4-14. Clock Test Mode Options

SEL_ECP_PIN = CLKTEST[3-0]	SIGNAL ON ECLK		SEL_GIO_PIN = CLKTEST[11-8]	SIGNAL ON N2HET1[12]
0000	Oscillator		0000	Oscillator Valid Status
0001	Main PLL free-running clock output		0001	Main PLL Valid status
0010	Reserved		0010	Reserved
0011	EXTCLKIN1		0011	Reserved
0100	CLK80K		0100	Reserved
0101	CLK10M		0101	CLK10M Valid status
0110	Secondary PLL free-running clock output		0110	Secondary PLL Valid Status
0111	EXTCLKIN2		0111	Reserved
1000	GCLK		1000	CLK80K
1001	RTI Base		1001	Reserved
1010	Reserved		1010	Reserved
1011	VCLKA1		1011	Reserved
1100	Reserved		1100	Reserved
1101	VCLKA3		1101	Reserved
1110	VCLKA4		1110	Reserved
1111	Reserved		1111	Reserved

4.7 Clock Monitoring

The LPO Clock Detect (LPOCLKDET) module consists of a clock monitor (CLKDET) and an internal low power oscillator (LPO).

The LPO provides two different clock sources – a low frequency (CLK80K) and a high frequency (CLK10M).

The CLKDET is a supervisor circuit for an externally supplied clock signal (OSCIN). In case the OSCIN frequency falls out of a frequency window, the CLKDET flags this condition in the global status register (GLBSTAT bit 0: OSC FAIL) and switches all clock domains sourced by OSCIN to the CLK10M clock (limp mode clock).

The valid OSCIN frequency range is defined as: $f_{CLK10M} / 4 < f_{OSCIN} < f_{CLK10M} * 4$.

4.7.1 Clock Monitor Timings

Table 4-15. LPO and Clock Detection

Parameter		MIN	Type	MAX	Unit
Clock Detection	oscillator fail frequency - lower threshold, using untrimmed LPO output	1.375	2.4	4.875	MHz
	oscillator fail frequency - higher threshold, using untrimmed LPO output	22	38.4	78	MHz
LPO - HF oscillator	untrimmed frequency	5.5	9.6	19.5	MHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900ms)			10	µs
	cold startup time			900	µs
	ICC, CLK10M and CLK80K active			150	µA
LPO - LF oscillator	untrimmed frequency	36	85	180	kHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900ms)			100	µs
	cold startup time			2000	µs
	ICC, only CLK80K active			27	µA
LPO	total ICC STANDBY current			20	µA

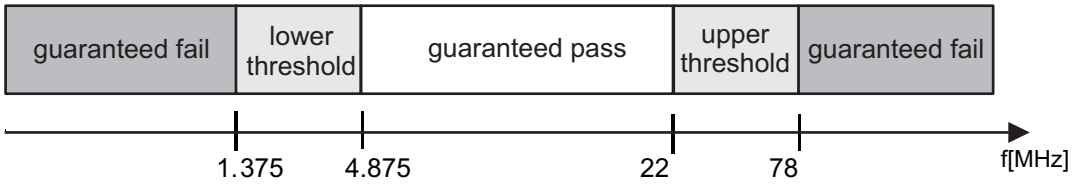

Figure 4-8. LPO and Clock Detection, Untrimmed CLK10M

4.7.2 External Clock (ECLK) Output Functionality

The ECLK pin can be configured to output a pre-scaled clock signal indicative of an internal device clock. This output can be externally monitored as a safety diagnostic.

4.7.3 Dual Clock Comparators

The Dual Clock Comparator (DCC) module determines the accuracy of selectable clock sources by counting the pulses of two independent clock sources (counter 0 and counter 1). If one clock is out of spec, an error signal is generated. For example, the DCC1 can be configured to use CLK10M as the reference clock (for counter 0) and VCLK as the "clock under test" (for counter 1). This configuration allows the DCC1 to monitor the PLL output clock when VCLK is using the PLL output as its source.

An additional use of this module is to measure the frequency of a selectable clock source, using the input clock as a reference, by counting the pulses of two independent clock sources. Counter 0 generates a fixed-width counting window after a preprogrammed number of pulses. Counter 1 generates a fixed-width pulse (1 cycle) after a pre-programmed number of pulses. This pulse sets as an error signal if counter 1 does not reach 0 within the counting window generated by counter 0.

4.7.3.1 Features

- Takes two different clock sources as input to two independent counter blocks.
- One of the clock sources is the known-good, or reference clock; the second clock source is the "clock under test."
- Each counter block is programmable with initial, or seed values.
- The counter blocks start counting down from their seed values at the same time; a mismatch from the expected frequency for the clock under test generates an error signal which is used to interrupt the CPU.

4.7.3.2 Mapping of DCC Clock Source Inputs

Table 4-16. DCC1 Counter 0 Clock Sources

CLOCK SOURCE [3:0]	CLOCK NAME
others	oscillator (OSCIN)
0x5	high frequency LPO
0xA	test clock (TCK)

Table 4-17. DCC1 Counter 1 Clock Sources

KEY [3:0]	CLOCK SOURCE [3:0]	CLOCK NAME
others	-	N2HET1[31]
0xA	0x0	Main PLL free-running clock output
	0x1	reserved
	0x2	low frequency LPO
	0x3	high frequency LPO
	0x4	flash HD pump oscillator
	0x5	EXTCLKIN1
	0x6	EXTCLKIN2
	0x7	ring oscillator
	0x8 - 0xF	VCLK

Table 4-18. DCC2 Counter 0 Clock Sources

CLOCK SOURCE [3:0]	CLOCK NAME
others	oscillator (OSCIN)
0xA	test clock (TCK)

Table 4-19. DCC2 Counter 1 Clock Sources

KEY [3:0]	CLOCK SOURCE [3:0]	CLOCK NAME
others	-	N2HET2[0]
0xA	00x0 - 0x7	Reserved
	0x8 - 0xF	VCLK

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4.8 Glitch Filters

A glitch filter is present on the following signals.

Table 4-20. Glitch Filter Timing Specifications

Pin	Parameter		MIN	MAX	Unit
nPORRST	tf(nPORRST)	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset(1)	500	2000	ns
nRST	tf(nRST)	Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	500	2000	ns
TEST	tf(TEST)	Filter time TEST pin; pulses less than MIN will be filtered out, pulses greater than MAX will pass through	500	2000	ns

(1) The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, etc.) without also generating a valid reset signal to the CPU.

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4.9 Device Memory Map

4.9.1 Memory Map Diagram

The figure below shows the device memory map.

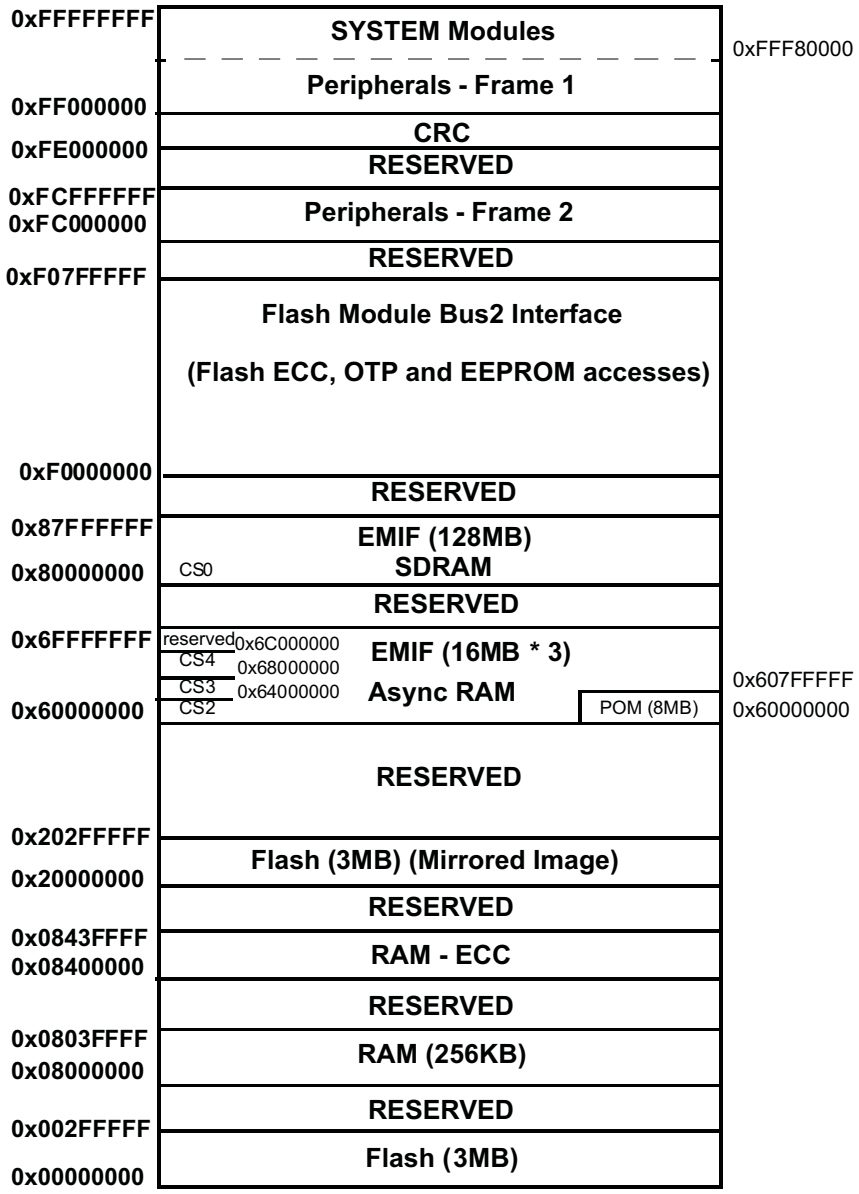

Figure 4-9. Memory Map

The Flash memory is mirrored to support ECC logic testing. The base address of the mirrored Flash image is 0x2000 0000.

4.9.2 Memory Map Table

Please refer to and for a block diagrams showing the devices interconnect.

Table 4-21. Device Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
Memories tightly coupled to the ARM Cortex-R4F CPU						
TCM Flash	CS0	0x0000_0000	0x00FF_FFFF	16MB	2MB/ 3MB	Abort
TCM RAM + RAM ECC	CSRAM0	0x0800_0000	0x0BFF_FFFF	64MB	256KB	
Mirrored Flash	Flash mirror frame	0x2000_0000	0x20FF_FFFF	16MB	3MB	
External Memory Accesses						
EMIF Chip Select 2 (asynchronous)	EMIF select 2	0x6000_0000	0x63FF_FFFF	64MB	16MB	Access to "Reserved" space will generate Abort
EMIF Chip Select 3 (asynchronous)	EMIF select 3	0x6400_0000	0x67FF_FFFF	64MB	16MB	
EMIF Chip Select 4 (asynchronous)	EMIF select 4	0x6800_0000	0x6BFF_FFFF	64MB	16MB	
EMIF Chip Select 0 (synchronous)	EMIF select 0	0x8000_0000	0x87FF_FFFF	128MB	128MB	
Flash Module Bus2 Interface						
Customer OTP, TCM Flash Banks		0xF000_0000	0xF000_FFFF	64KB	16KB	Abort
Customer OTP, EEPROM Bank		0xF000_E000	0xF000_FFFF	8KB	4KB	
Customer OTP–ECC, TCM Flash Banks		0xF004_0000	0xF004_1FFF	8KB	2KB	
Customer OTP–ECC, EEPROM Bank		0xF004_1C00	0xF004_1FFF	1KB	1KB	
TI OTP, TCM Flash Banks		0xF008_0000	0xF008_FFFF	64KB	16KB	
TI OTP, EEPROM Bank		0xF008_E000	0xF008_FFFF	8KB	4KB	
TI OTP–ECC, TCM Flash Banks		0xF00C_0000	0xF00C_1FFF	8KB	2KB	
TI OTP–ECC, EEPROM Bank		0xF00C_1C00	0xF00C_1FFF	1KB	1KB	
EEPROM Bank–ECC		0xF010_0000	0xF013_FFFF	256KB	8KB	
EEPROM Bank		0xF020_0000	0xF03F_FFFF	2MB	64KB	
Flash Data Space ECC		0xF040_0000	0xF04F_FFFF	1MB	384KB	
Ethernet and EMIF slave interfaces						
CPPI Memory Slave (Ethernet RAM)		0xFC52_0000	0xFC52_1FFF	8KB	8KB	Abort
CPGMAC Slave (Ethernet Slave)		0xFCF7_8000	0xFCF7_87FF	2KB	2KB	No error
CPGMACSS Wrapper (Ethernet Wrapper)		0xFCF7_8800	0xFCF7_88FF	256B	256B	No error
EMIF Registers		0xFCFF_E800	0xFCFF_E8FF	256B	256B	Abort

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Table 4-21. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
Cyclic Redundancy Checker (CRC) Module Registers						
CRC	CRC frame	0xFE00_0000	0xFEFF_FFFF	16MB	512B	Accesses above 0x200 generate abort.
Peripheral Memories						
MIBSPI5 RAM	PCS[5]	0xFF0A_0000	0xFF0B_FFFF	128KB	2KB	Abort for accesses above 2KB
MIBSPI3 RAM	PCS[6]	0xFF0C_0000	0xFF0D_FFFF	128KB	2KB	Abort for accesses above 2KB
MIBSPI1 RAM	PCS[7]	0xFF0E_0000	0xFF0F_FFFF	128KB	2KB	Abort for accesses above 2KB
DCAN3 RAM	PCS[13]	0xFF1A_0000	0xFF1B_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
DCAN2 RAM	PCS[14]	0xFF1C_0000	0xFF1D_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
DCAN1 RAM	PCS[15]	0xFF1E_0000	0xFF1F_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
MIBADC2 RAM	PCS[29]	0xFF3A_0000	0xFF3B_FFFF	128KB	8KB	Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF.
MIBADC1 RAM	PCS[31]	0xFF3E_0000	0xFF3F_FFFF	128KB	8KB	Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF.
N2HET2 RAM	PCS[34]	0xFF44_0000	0xFF45_FFFF	128KB	16KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF.
N2HET1 RAM	PCS[35]	0xFF46_0000	0xFF47_FFFF	128KB	16KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF.
N2HET2 TU2 RAM	PCS[38]	0xFF4C_0000	0xFF4D_FFFF	128KB	1KB	Abort
N2HET1 TU1 RAM	PCS[39]	0xFF4E_0000	0xFF4F_FFFF	128KB	1KB	Abort
Debug Components						
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4F Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect
ETM-R4	CSCS2	0xFFA0_2000	0xFFA0_2FFF	4KB	4KB	Reads return zeros, writes have no effect
CoreSight TPIU	CSCS3	0xFFA0_3000	0xFFA0_3FFF	4KB	4KB	Reads return zeros, writes have no effect
POM	CSCS4	0xFFA0_4000	0xFFA0_4FFF	4KB	4KB	Abort
Peripheral Control Registers						
HTU1	PS[22]	0xFFF7_A400	0xFFF7_A4FF	256B	256B	Reads return zeros, writes have no effect
HTU2	PS[22]	0xFFF7_A500	0xFFF7_A5FF	256B	256B	Reads return zeros, writes have no effect
N2HET1	PS[17]	0xFFF7_B800	0xFFF7_B8FF	256B	256B	Reads return zeros, writes have no effect

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Table 4-21. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
N2HET2	PS[17]	0xFFF7_B900	0xFFF7_B9FF	256B	256B	Reads return zeros, writes have no effect
GIO	PS[16]	0xFFF7_BC00	0xFFF7_BCFF	256B	256B	Reads return zeros, writes have no effect
MIBADC1	PS[15]	0xFFF7_C000	0xFFF7_C1FF	512B	512B	Reads return zeros, writes have no effect
MIBADC2	PS[15]	0xFFF7_C200	0xFFF7_C3FF	512B	512B	Reads return zeros, writes have no effect
I2C	PS[10]	0xFFF7_D400	0xFFF7_D4FF	256B	256B	Reads return zeros, writes have no effect
DCAN1	PS[8]	0xFFF7_DC00	0xFFF7_DDFF	512B	512B	Reads return zeros, writes have no effect
DCAN2	PS[8]	0xFFF7_DE00	0xFFF7_DFFF	512B	512B	Reads return zeros, writes have no effect
DCAN3	PS[7]	0xFFF7_E000	0xFFF7_E1FF	512B	512B	Reads return zeros, writes have no effect
LIN	PS[6]	0xFFF7_E400	0xFFF7_E4FF	256B	256B	Reads return zeros, writes have no effect
SCI	PS[6]	0xFFF7_E500	0xFFF7_E5FF	256B	256B	Reads return zeros, writes have no effect
MibSPI1	PS[2]	0xFFF7_F400	0xFFF7_F5FF	512B	512B	Reads return zeros, writes have no effect
SPI2	PS[2]	0xFFF7_F600	0xFFF7_F7FF	512B	512B	Reads return zeros, writes have no effect
MibSPI3	PS[1]	0xFFF7_F800	0xFFF7_F9FF	512B	512B	Reads return zeros, writes have no effect
SPI4	PS[1]	0xFFF7_FA00	0xFFF7_FBFF	512B	512B	Reads return zeros, writes have no effect
MibSPI5	PS[0]	0xFFF7_FC00	0xFFF7_FDFF	512B	512B	Reads return zeros, writes have no effect
System Modules Control Registers and Memories						
DMA RAM	PPCS0	0xFFF8_0000	0xFFF8_0FFF	4KB	4KB	Abort
VIM RAM	PPCS2	0xFFF8_2000	0xFFF8_2FFF	4KB	1KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FF. Abort generated for accesses beyond 0x3FF.
RTP RAM	PPCS3	0xFFF8_3000	0xFFF8_3FFF	4KB	4KB	Abort
Flash Module	PPCS7	0xFFF8_7000	0xFFF8_7FFF	4KB	4KB	Abort
eFuse Controller	PPCS12	0xFFF8_C000	0xFFF8_CFFF	4KB	4KB	Abort
Power Management Module (PMM)	PPSE0	0xFFFF_0000	0xFFFF_01FF	512B	512B	Abort
Test Controller (FMTM)	PPSE1	0xFFFF_0400	0xFFFF_07FF	1KB	1KB	Reads return zeros, writes have no effect
PCR registers	PPS0	0xFFFF_E000	0xFFFF_E0FF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 2 (see device TRM)	PPS0	0xFFFF_E100	0xFFFF_E1FF	256B	256B	Reads return zeros, writes have no effect
PBIST	PPS1	0xFFFF_E400	0xFFFF_E5FF	512B	512B	Reads return zeros, writes have no effect
STC	PPS1	0xFFFF_E600	0xFFFF_E6FF	256B	256B	Generates address error interrupt, if enabled

Table 4-21. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
IOMM Multiplexing Control Module	PPS2	0xFFFF_EA00	0xFFFF_EBFF	512B	512B	Reads return zeros, writes have no effect
DCC1	PPS3	0xFFFF_EC00	0xFFFF_ECFF	256B	256B	Reads return zeros, writes have no effect
DMA	PPS4	0xFFFF_F000	0xFFFF_F3FF	1KB	1KB	Reads return zeros, writes have no effect
DCC2	PPS5	0xFFFF_F400	0xFFFF_F4FF	256B	256B	Reads return zeros, writes have no effect
ESM	PPS5	0xFFFF_F500	0xFFFF_F5FF	256B	256B	Reads return zeros, writes have no effect
CCMR4	PPS5	0xFFFF_F600	0xFFFF_F6FF	256B	256B	Reads return zeros, writes have no effect
DMM	PPS5	0xFFFF_F700	0xFFFF_F7FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC even	PPS6	0xFFFF_F800	0xFFFF_F8FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC odd	PPS6	0xFFFF_F900	0xFFFF_F9FF	256B	256B	Reads return zeros, writes have no effect
RTP	PPS6	0xFFFF_FA00	0xFFFF_FAFF	256B	256B	Reads return zeros, writes have no effect
RTI + DWWD	PPS7	0xFFFF_FC00	0xFFFF_FCFF	256B	256B	Reads return zeros, writes have no effect
VIM Parity	PPS7	0xFFFF_FD00	0xFFFF_FDFF	256B	256B	Reads return zeros, writes have no effect
VIM	PPS7	0xFFFF_FE00	0xFFFF_FEFF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 1 (see device TRM)	PPS7	0xFFFF_FF00	0xFFFF_FFFF	256B	256B	Reads return zeros, writes have no effect

4.9.3 Master/Slave Access Privileges

The table below lists the access permissions for each bus master on the device. A bus master is a module that can initiate a read or a write transaction on the device.

Each slave module on the main interconnect is listed in the table. A "Yes" indicates that the module listed in the "MASTERS" column can access that slave module.

Table 4-22. Master / Slave Access Matrix

MASTERS	ACCESS MODE	SLAVES ON MAIN SCR				
		Flash Module Bus2 Interface: OTP, ECC, EEPROM Bank	Non-CPU Accesses to Program Flash and CPU Data RAM	CRC	EMIF, Ethernet, Slave Interfaces	Peripheral Control Registers, All Peripheral Memories, And All System Module Control Registers And Memories
CPU READ	User/Privilege	Yes	Yes	Yes	Yes	Yes
CPU WRITE	User/Privilege	No	Yes	Yes	Yes	Yes
DMA	User	Yes	Yes	Yes	Yes	Yes
POM	User	Yes	Yes	Yes	Yes	Yes
DMM	User	Yes	Yes	Yes	Yes	Yes
DAP	Privilege	Yes	Yes	Yes	Yes	Yes
HTU1	Privilege	No	Yes	Yes	Yes	Yes
HTU2	Privilege	No	Yes	Yes	Yes	Yes
EMAC	User	No	Yes	No	Yes	No

4.9.3.1 Special Notes on Accesses to Certain Slaves

Write accesses to the Power Domain Management Module (PMM) control registers are limited to the CPU (master id = 1). The other masters can only read from these registers.

A debugger can also write to the PMM registers. The master-id check is disabled in debug mode.

The device contains dedicated logic to generate a bus error response on any access to a module that is in a power domain that has been turned OFF.

4.9.4 POM Overlay Considerations

- The POM overlay can map onto up to 8MB of the internal or external memory space. The starting address and the size of the memory overlay are configurable via the POM module control registers. Care must be taken to ensure that the overlay is mapped on to available memory.
- ECC must be disabled by software via CP15 in case POM overlay is enabled; otherwise ECC errors will be generated.
- POM overlay must not be enabled when the flash and internal RAM memories are swapped via the MEM SWAP field of the Bus Matrix Module Control Register 1 (BMMCR1).
- When POM is used to overlay the flash on to internal or external RAM, there is a bus contention possibility when another master accesses the TCM flash. This results in a system hang.
  - The POM module implements a timeout feature to detect this exact scenario. The timeout needs to be enabled whenever POM overlay is enabled.
  - The timeout can be enabled by writing 1010 to the Enable TimeOut (ETO) field of the POM Global Control register (POMGLBCTRL, address = 0xFFA04000).
  - In case a read request by the POM cannot be completed within 32 HCLK cycles, the timeout (TO) flag is set in the POM Flag register (POMFLG, address = 0xFFA0400C). Also, an abort is generated to the CPU. This can be a prefetch abort for an instruction fetch or a data abort for a data fetch.
  - The prefetch- and data-abort handlers must be modified to check if the TO flag in the POM module is set. If so, then the application can assume that the timeout is caused by a bus contention between the POM transaction and another master accessing the same memory region. The abort handlers need to clear the TO flag, so that any further aborts are not misinterpreted as having been caused due to a timeout from the POM.

4.10 Flash Memory

4.10.1 Flash Memory Configuration

Flash Bank: A separate block of logic consisting of 1 to 16 sectors. Each flash bank normally has a customer-OTP and a TI-OTP area. These flash sectors share input/output buffers, data paths, sense amplifiers, and control logic.

Flash Sector: A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.

Flash Pump: A charge pump which generates all the voltages required for reading, programming, or erasing the flash banks.

Flash Module: Interface circuitry required between the host CPU and the flash banks and pump module.

Table 4-23. Flash Memory Banks and Sectors

Memory Arrays (or Banks)(1)	Sector No.	Segment	Low Address	High Address
BANK0 (1.5MBytes)	0	32K Bytes	0x0000_0000	0x0000_7FFF
	1	32K Bytes	0x0000_8000	0x0000_FFFF
	2	32K Bytes	0x0001_0000	0x0001_7FFF
	3	32K Bytes	0x0001_8000	0x0001_FFFF
	4	128K Bytes	0x0002_0000	0x0003_FFFF
	5	128K Bytes	0x0004_0000	0x0005_FFFF
	6	128K Bytes	0x0006_0000	0x0007_FFFF
	7	128K Bytes	0x0008_0000	0x0009_FFFF
	8	128K Bytes	0x000A_0000	0x000B_FFFF
	9	128K Bytes	0x000C_0000	0x000D_FFFF
	10	128K Bytes	0x000E_0000	0x000F_FFFF
	11	128K Bytes	0x0010_0000	0x0011_FFFF
	12	128K Bytes	0x0012_0000	0x0013_FFFF
	13	128K Bytes	0x0014_0000	0x0015_FFFF
	14	128K Bytes	0x0016_0000	0x0017_FFFF
BANK1 (1.5MBytes)	0	128K Bytes	0x0018_0000	0x0019_FFFF
	1	128K Bytes	0x001A_0000	0x001B_FFFF
	2	128K Bytes	0x001C_0000	0x001D_FFFF
	3	128K Bytes	0x001E_0000	0x001F_FFFF
	4	128K Bytes	0x0020_0000	0x0021_FFFF
	5	128K Bytes	0x0022_0000	0x0023_FFFF
	6	128K Bytes	0x0024_0000	0x0025_FFFF
	7	128K Bytes	0x0026_0000	0x0027_FFFF
	8	128K Bytes	0x0028_0000	0x0029_FFFF
	9	128K Bytes	0x002A_0000	0x002B_FFFF
	10	128K Bytes	0x002C_0000	0x002D_FFFF
	11	128K Bytes	0x002E_0000	0x002F_FFFF
BANK7 (64kBytes) for EEPROM emulation(2)(3)	0	16K Bytes	0xF020_0000	0xF020_3FFF
	1	16K Bytes	0xF020_4000	0xF020_7FFF
	2	16K Bytes	0xF020_8000	0xF020_BFFF
	3	16K Bytes	0xF020_C000	0xF020_FFFF

(1) The Flash banks are 144-bit wide bank with ECC support.
(2) The flash bank7 can be programmed while executing code from flash bank0 or bank1.
(3) Code execution is not allowed from flash bank7.

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4.10.2 Main Features of Flash Module

- Support for multiple flash banks for program and/or data storage
- Simultaneous read access on a bank while performing program or erase operation on any other bank
- Integrated state machines to automate flash erase and program operations
- Software interface for flash program and erase operations
- Pipelined mode operation to improve instruction access interface bandwidth
- Support for Single Error Correction Double Error Detection (SECDED) block inside Cortex-R4F CPU
  - Error address is captured for host system debugging
- Support for a rich set of diagnostic features

4.10.3 ECC Protection for Flash Accesses

All accesses to the program flash memory are protected by Single Error Correction Double Error Detection (SECDED) logic embedded inside the CPU. The flash module provides 8 bits of ECC code for 64 bits of instructions or data fetched from the flash memory. The CPU calculates the expected ECC code based on the 64 bits received and compares it with the ECC code returned by the flash module. A signle-bit error is corrected and flagged by the CPU, while a multi-bit error is only flagged. The CPU signals an ECC error via its Event bus. This signaling mechanism is not enabled by default and must be enabled by setting the "X" bit of the Performance Monitor Control Register, c9.

```
MRC p15,#0,r1,c9,c12,#0    ;Enabling Event monitor states
ORR r1, r1, #0x00000010
MCR p15,#0,r1,c9,c12,#0    ;Set 4th bit (‘X’) of PMNC register
MRC p15,#0,r1,c9,c12,#0
```

The application must also explicitly enable the CPU's ECC checking for accesses on the CPU's ATCM and BTCM interfaces. These are connected to the program flash and data RAM respectively. ECC checking for these interfaces can be done by setting the B1TCMPCEN, B0TCMPCEN and ATCMPCEN bits of the System Control coprocessor's Auxiliary Control Register, c1.

```
MRC p15, #0, r1, c1, c0, #1
ORR r1, r1, #0x0e000000        ;Enable ECC checking for ATCM and BTCMs
DMB
MCR p15, #0, r1, c1, c0, #1
```

4.10.4 Flash Access Speeds

For information on flash memory access speeds and the relevant wait states required, refer to Section 3.4.

4.10.5 Flash Program and Erase Timings

Table 4-24. Timing Specifications for Flash

Parameter			MIN	NOM	MAX	Unit
t_{prog} (144bit)	Wide Word (144bit) programming time			40	tbd	µs
t_{prog} (Total)	3MByte programming time(1)	-40°C to 125°C			tbd	s
		0°C to 60°C, for first 25 cycles		8	tbd	s
t_{prog} (Total)	EEPROM Emulation 64kByte programming time(1)	-40°C to 12°5C			tbd	ms
		0°C to 60°C, for first 25 cycles		165	tbd	ms
t_{erase} (sector)	Sector erase time	-40°C to 125°C			tbd	ms
		0°C to 60°C, for first 25 cycles		30	tbd	ms
t_{erase} (bank)	Bank erase time(2)	Flash Bank 0		300	tbd	ms
t_{erase} (bank)	Bank erase time(2)	Flash Bank 1		240	tbd	ms
t_{erase} (bank)	EEPROM Emulation Bank erase time(2)	Flash Bank 7		80	tbd	ms
t_{wec}	Write/erase cycles	Flash Bank 0 Flash Bank 1			1000	cycles
t_{wec}	Write/erase cycles	Flash Bank 7			100000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time.
(2) Nominal conditions for the above specifications mean the first 25 program / erase cycles at an ambient temperature between 0c to 60c

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4.11 Tightly-Coupled RAM Interface Module

Figure 4-10 illustrates the connection of the Tightly Coupled RAM (TCRAM) to the Cortex-R4F™ CPU.

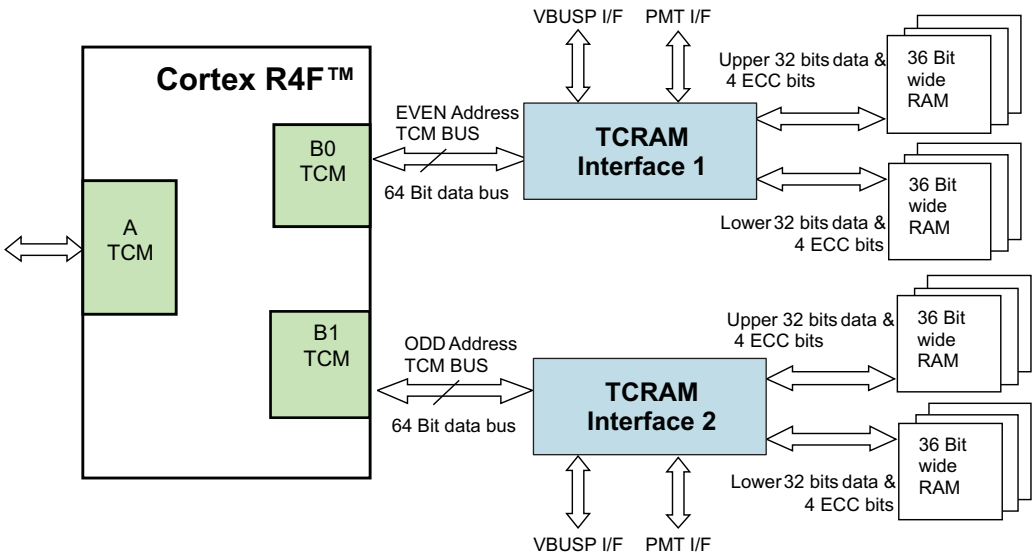

Figure 4-10. TCRAM Block Diagram

4.11.1 Features

The features of the Tightly Coupled RAM (TCRAM) Module are:

- Acts as slave to the Cortex-R4F CPU's BTCM interface
- Supports CPU's internal ECC scheme by providing 64-bit data and 8-bit ECC code
- Monitors CPU Event Bus and generates single or multi-bit error interrupts
- Stores addresses for single and multi-bit errors
- Supports RAM trace module
- Provides CPU address bus integrity checking by supporting parity checking on the address bus
- Performs redundant address decoding for the RAM bank chip select and ECC select generation logic
- Provides enhanced safety for the RAM addressing by implementing two 36-bit wide byte-interleaved RAM banks and generating independent RAM access control signals to the two banks
- Supports auto-initialization of the RAM banks along with the ECC bits

4.11.2 TCRAMW ECC Support

The TCRAMW passes on the ECC code for each data read by the Cortex-R4F CPU from the RAM. It also stores the CPU's ECC port contents in the ECC RAM when the CPU does a write to the RAM. The TCRAMW monitors the CPU's event bus and provides registers for indicating single/multi-bit errors and also for identifying the address that caused the single or multi-bit error. The event signaling and the ECC checking for the RAM accesses must be enabled inside the CPU.

For more information see the RM48x Technical Reference Manual (SPNU481).

4.12 Parity Protection for Accesses to peripheral RAMs

Accesses to all peripheral RAMs are protected by odd/even parity checking. During a read access the parity is calculated based on the data read from the peripheral RAM and compared with the good parity value stored in the parity RAM for that peripheral. If any word fails the parity check, the module generates a parity error signal that is mapped to the Error Signaling Module. The module also captures the peripheral RAM address that caused the parity error.

The parity protection for peripheral RAMs is not enabled by default and must be enabled by the application. Each individual peripheral contains control registers to enable the parity protection for accesses to its RAM.

NOTE

The CPU read access gets the actual data from the peripheral. The application can choose to generate an interrupt whenever a peripheral RAM parity error is detected.

4.13 On-Chip SRAM Initialization and Testing

4.13.1 On-Chip SRAM Self-Test Using PBIST

4.13.1.1 Features

- Extensive instruction set to support various memory test algorithms
- ROM-based algorithms allow application to run TI production-level memory tests
- Independent testing of all on-chip SRAM

4.13.1.2 PBIST RAM Groups

Table 4-25. PBIST RAM Grouping

Memory	RAM Group	Test Clock	MEM Type	Test Pattern (Algorithm)			
				triple read slow read	triple read fast read	March 13N(1) two port (cycles)	March 13N(1) single port (cycles)
				ALGO MASK 0x1	ALGO MASK 0x2	ALGO MASK 0x4	ALGO MASK 0x8
PBIST_ROM	1	ROM CLK	ROM	X	X		
STC_ROM	2	ROM CLK	ROM	X	X		
DCAN1	3	VCLK	Dual Port			25200	
DCAN2	4	VCLK	Dual Port			25200	
DCAN3	5	VCLK	Dual Port			25200	
ESRAM1	6	HCLK	Single Port				266280
MIBSPI1	7	VCLK	Dual Port			33440	
MIBSPI3	8	VCLK	Dual Port			33440	
MIBSPI5	9	VCLK	Dual Port			33440	
VIM	10	VCLK	Dual Port			12560	
MIBADC1	11	VCLK	Dual Port			4200	
DMA	12	HCLK	Dual Port			18960	
N2HET1	13	VCLK	Dual Port			31680	
HET TU1	14	VCLK	Dual Port			6480	
RTP	15	HCLK	Dual Port			37800	
MIBADC2	18	VCLK	Dual Port			4200	
N2HET2	19	VCLK	Dual Port			31680	
HET TU2	20	VCLK	Dual Port			6480	
ESRAM5	21	HCLK	Single Port				266280
ESRAM6	22	HCLK	Single Port				266280
ETHERNET	23	VCLK3	Dual Port			8700	
	24					6360	
	25		Single Port				133160
ESRAM8	28	HCLK	Single Port				266280

(1) There are several memory testing algorithms stored in the PBIST ROM. However, TI recommends the March13N algorithm for application testing.

The PBIST ROM clock frequency is limited to 100MHz, if 100MHz < HCLK <= HCLKmax, or HCLK, if HCLK <= 100MHz.

The PBIST ROM clock is divided down from HCLK. The divider is selected by programming the ROM_DIV field of the Memory Self-Test Global Control Register (MSTGCR) at address 0xFFFFFF58.

4.13.2 On-Chip SRAM Auto Initialization

This microcontroller allows some of the on-chip memories to be initialized via the Memory Hardware Initialization mechanism in the System module. This hardware mechanism allows an application to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC).

The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized.

For more information on these registers see the RM48x Technical Reference Manual (SPNU481).

The mapping of the different on-chip memories to the specific bits of the MSINENA registers is shown in Table 4-26.

Table 4-26. Memory Initialization

CONNECTING MODULE	ADDRESS RANGE		MSINENA REGISTER BIT #
	BASE ADDRESS	ENDING ADDRESS	
RAM (PD#1)	0x08000000	0x0800FFFF	0(1)
RAM (RAM_PD#1)	0x08010000	0x0801FFFF	0(1)
RAM (RAM_PD#2)	0x08020000	0x0802FFFF	0(1)
RAM (RAM_PD#3)	0x08030000	0x0803FFFF	0(1)
MIBSPI5 RAM	0xFF0A0000	0xFF0BFFFF	12(2)
MIBSPI3 RAM	0xFF0C0000	0xFF0DFFFF	11(2)
MIBSPI1 RAM	0xFF0E0000	0xFF0FFFFF	7(2)
DCAN3 RAM	0xFF1A0000	0xFF1BFFFF	10
DCAN2 RAM	0xFF1C0000	0xFF1DFFFF	6
DCAN1 RAM	0xFF1E0000	0xFF1FFFFF	5
MIBADC2 RAM	0xFF3A0000	0xFF3BFFFF	14
MIBADC1 RAM	0xFF3E0000	0xFF3FFFFF	8
N2HET2 RAM	0xFF440000	0xFF57FFFF	15
N2HET1 RAM	0xFF460000	0xFF47FFFF	3
HET TU2 RAM	0xFF4C0000	0xFF4DFFFF	16
HET TU1 RAM	0xFF4E0000	0xFF4FFFFF	4
DMA RAM	0xFFF80000	0xFFF80FFF	1
VIM RAM	0xFFF82000	0xFFF82FFF	2
Ethernet RAM (CPPI Memory Slave)	0xFC520000	0xFC521FFF	n/a

(1) The TCM RAM wrapper has separate control bits to select the RAM power domain that is to be auto-initialized.
(2) The MibSPIx modules perform an initialization of the transmit and receive RAMs as soon as the multi-buffered mode is enabled. This is independent of whether the application chooses to initialize the MibSPIx RAMs using the system module auto-initialization method.

4.14 External Memory Interface (EMIF)

4.14.1 Features

The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous memories or SDRAM devices. The EMIF features includes support for:

- 3 addressable chip select for asynchronous memories of up to 16MB each
- 1 addressable chip select space for SDRAMs up to 128MB
- 8 or 16-bit data bus width
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- Data bus parking

4.14.2 Electrical and Timing Specifications

4.14.2.1 Read Timing (Asynchronous RAM)

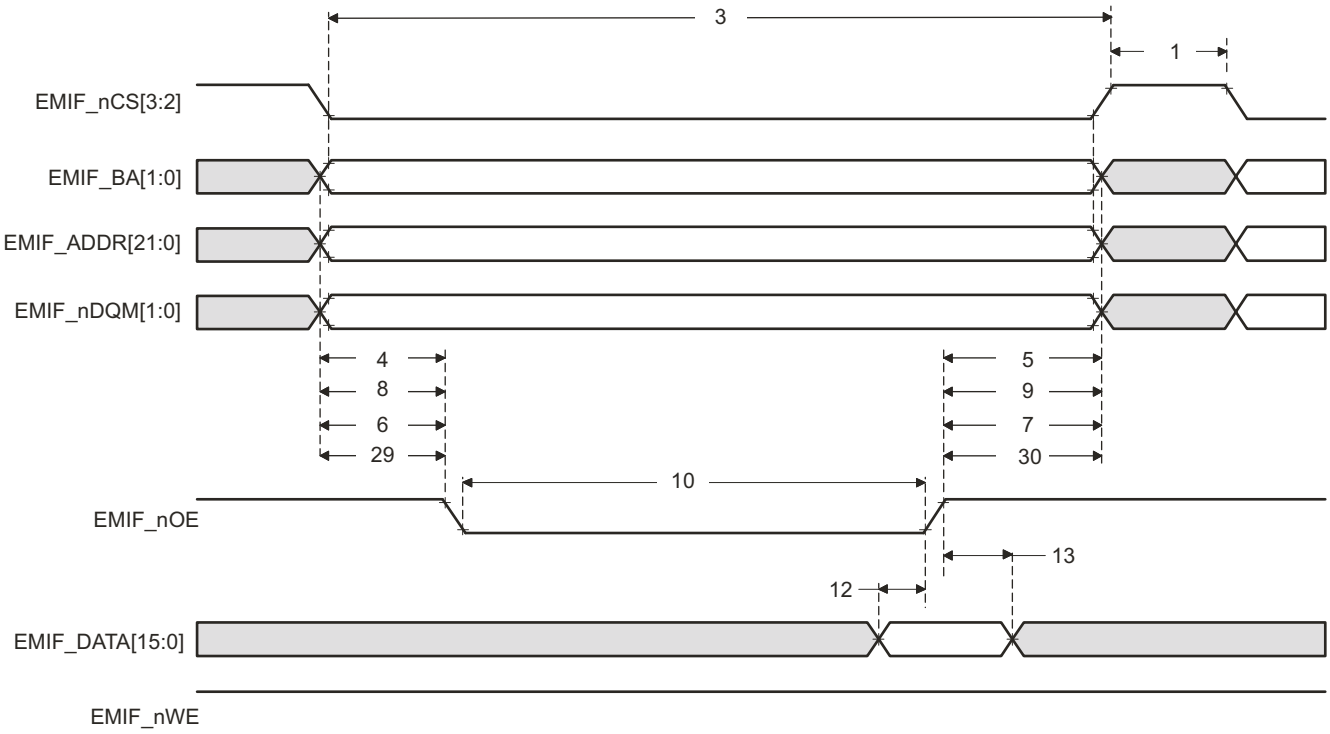

Figure 4-11. Asynchronous Memory Read Timing

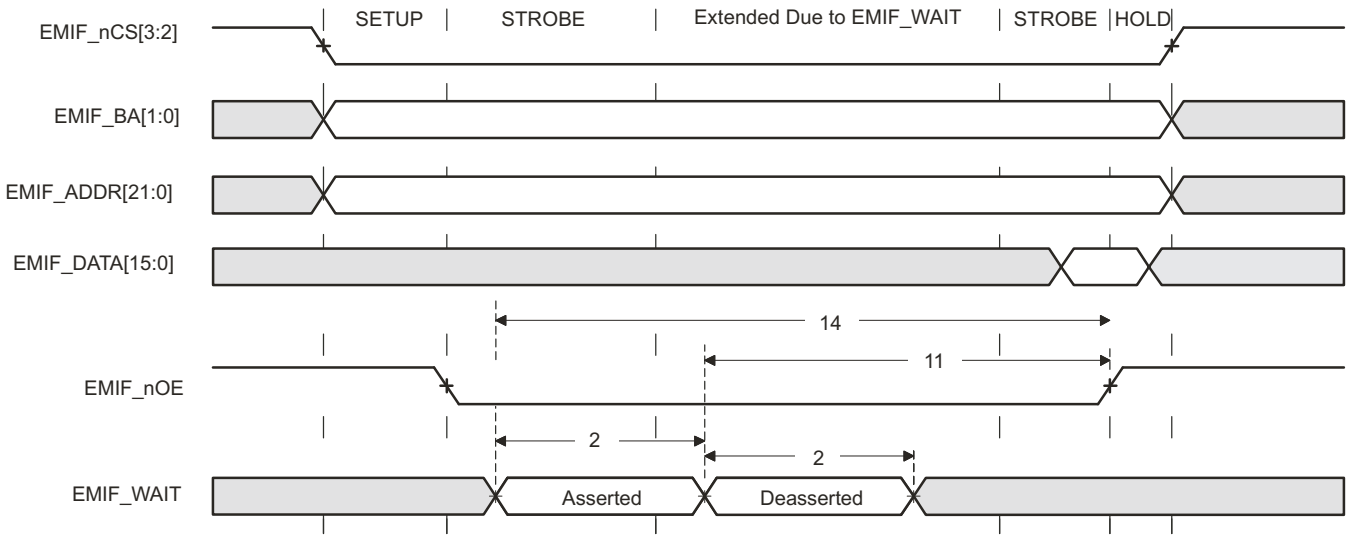

Figure 4-12. EMIFnWAIT Read Timing Requirements

4.14.2.2 Write Timing (Asynchronous RAM)

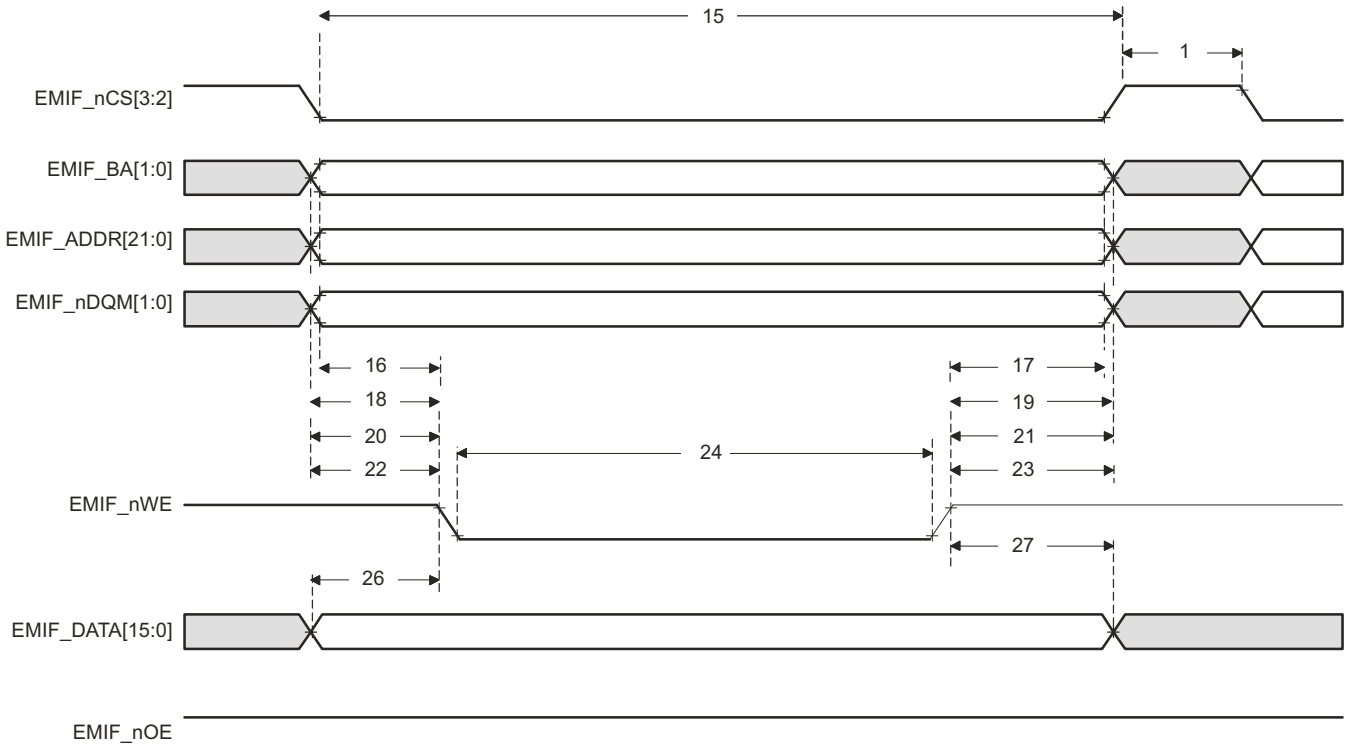

Figure 4-13. Asynchronous Memory Write Timing

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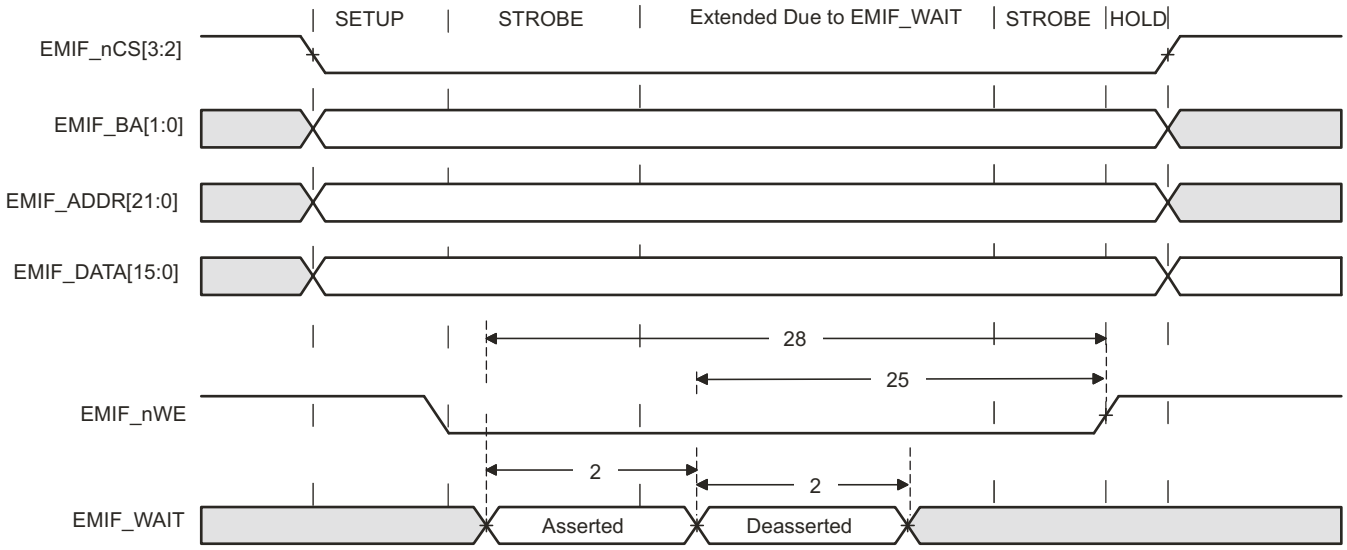

Figure 4-14. EMIFnWAIT Write Timing Requirements

4.14.2.3 Read Timing (Synchronous RAM)

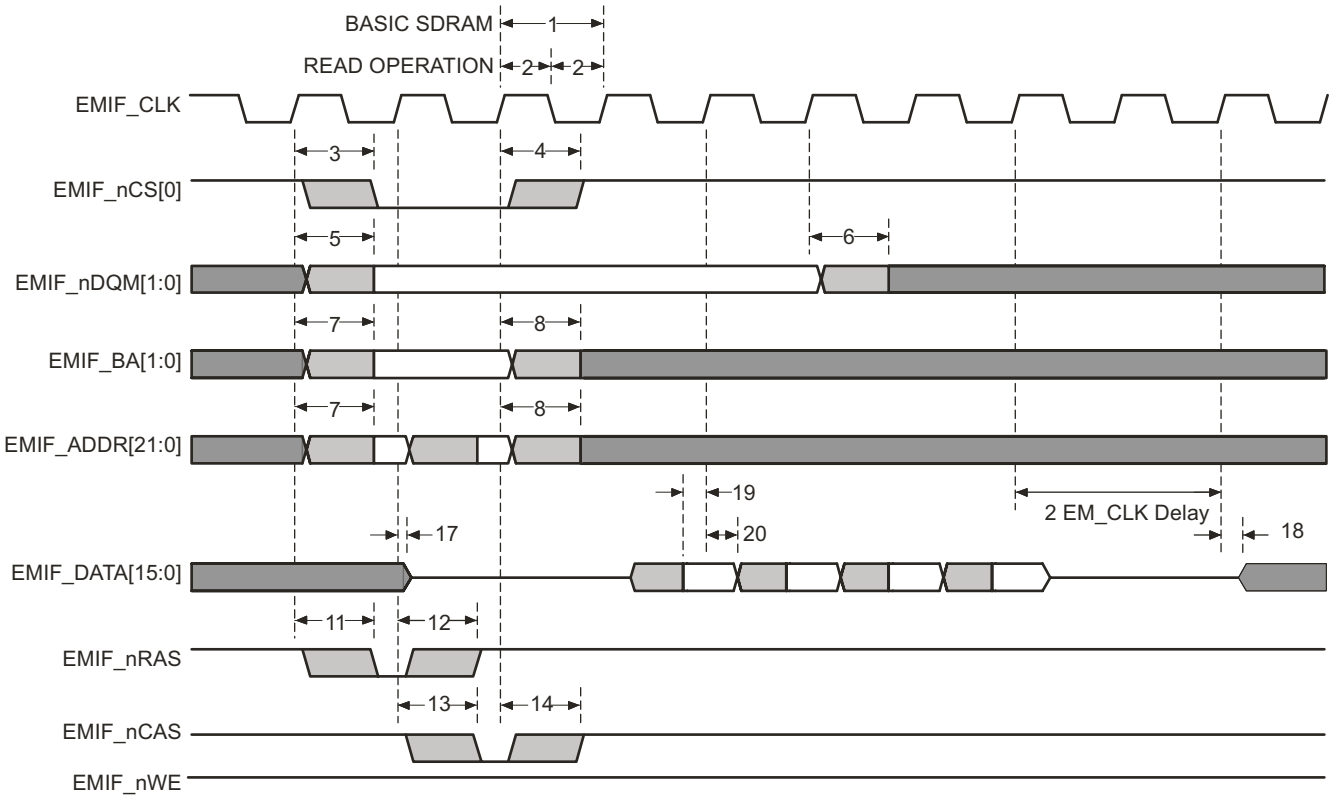

Figure 4-15. Basic SDRAM Read Operation

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4.14.2.4 Write Timing (Synchronous RAM)

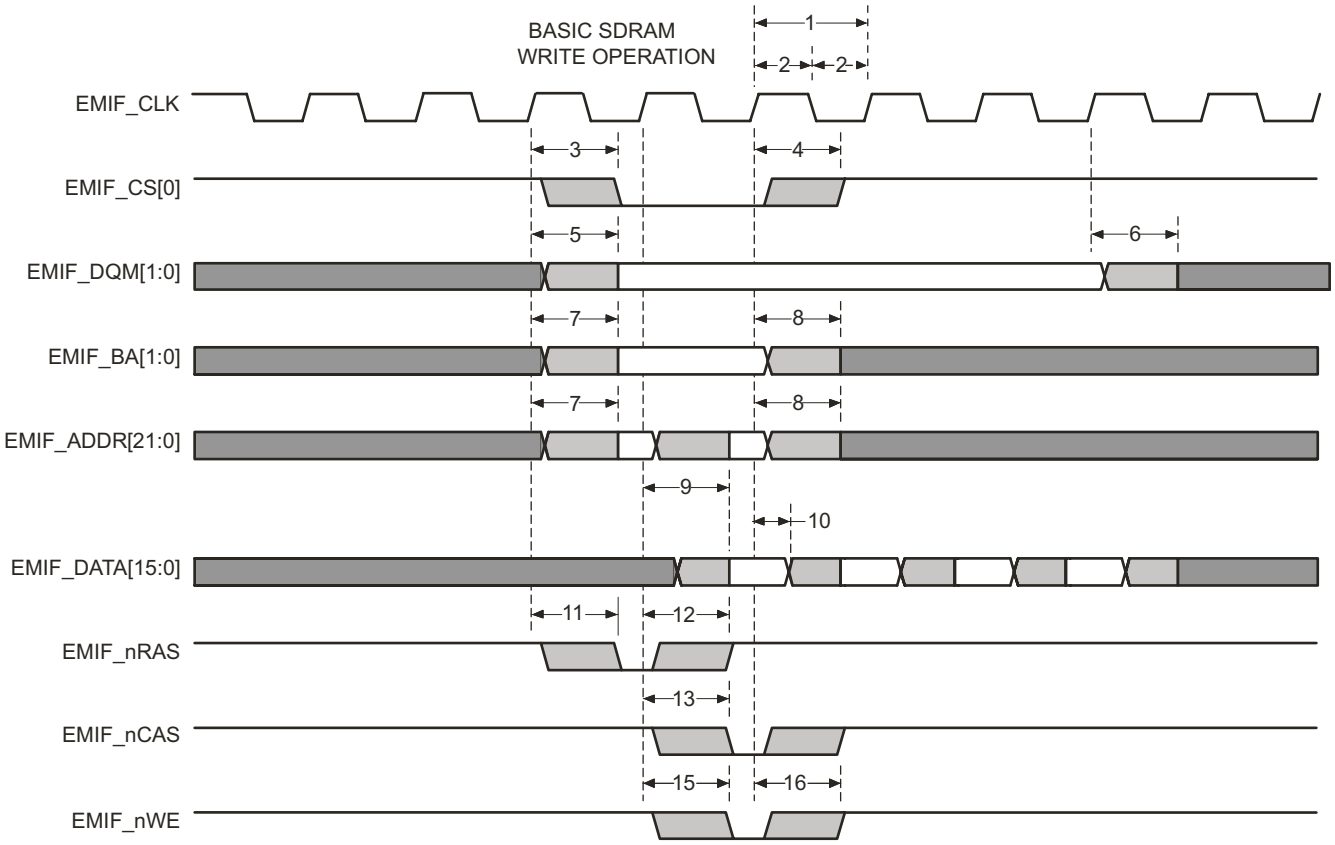

Figure 4-16. Basic SDRAM Write Operation

4.14.2.5 EMIF Asynchronous Memory Timing

Table 4-27. EMIF Asynchronous Memory Timing Requirements

NO.			Value			Unit
			MIN	NOM	MAX	
Reads and Writes						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EMIFnWAIT assertion and deassertion	2E			ns
Reads						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMIFDATA[15:0] valid before EMIFnOE high	3			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMIFDATA[15:0] valid after EMIFnOE high	0.5			ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMIFnWAIT asserted before end of Strobe Phase (1)	4E+3			ns
Writes						
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMIFnWAIT asserted before end of Strobe Phase (1)	4E+3			ns

(1) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMIFnWAIT must be asserted to add extended wait states. Figure Figure 4-12 and Figure Figure 4-14 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 4-28. EMIF Asynchronous Memory Switching Characteristics(1)(2)(3)

NO	Parameter		Value			Unit
			MIN	NOM	MAX	
Reads and Writes						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E -3	(TA)*E	(TA)*E + 3	ns
Reads						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E -3	(RS+RST+RH)*E	(RS+RST+RH)*E + 3	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E -3	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 3	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, EMIFnCS[4:2] low to EMIFnOE low (SS = 0)	(RS)*E-3	(RS)*E	(RS)*E+3	ns
		Output setup time, EMIFnCS[4:2] low to EMIFnOE low (SS = 1)	-3	0	+3	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, EMIFnOE high to EMIFnCS[4:2] high (SS = 0)	(RH)*E -3	(RH)*E	(RH)*E + 3	ns
		Output hold time, EMIFnOE high to EMIFnCS[4:2] high (SS = 1)	-3	0	+3	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMIFBA[1:0] valid to EMIFnOE low	(RS)*E-3	(RS)*E	(RS)*E+3	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, EMIFnOE high to EMIFBA[1:0] invalid	(RH)*E-3	(RH)*E	(RH)*E+3	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMIFADDR[21:0] valid to EMIFnOE low	(RS)*E-3	(RS)*E	(RS)*E+3	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, EMIFnOE high to EMIFADDR[21:0] invalid	(RH)*E-3	(RH)*E	(RH)*E+3	ns
10	$t_{w(EMOEL)}$	EMIFnOE active low width (EW = 0)	(RST)*E-3	(RST)*E	(RST)*E+3	ns
		EMIFnOE active low width (EW = 1)	(RST+(EWC*16)) *E-3	(RST+(EWC*16))*E	(RST+(EWC*16)) *E+3	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMIFnWAIT deasserted to EMIFnOE high	3E-3	4E	4E+3	ns
Writes						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)* E-3	(WS+WST+WH)*E	(WS+WST+WH)* E+3	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E -3	(WS+WST+WH+(E WC*16))*E	(WS+WST+WH+(EWC*16))*E + 3	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, EMIFnCS[4:2] low to EMIFnWE low (SS = 0)	(WS)*E -3	(WS)*E	(WS)*E + 3	ns
		Output setup time, EMIFnCS[4:2] low to EMIFnWE low (SS = 1)	-3	0	+3	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, EMIFnWE high to EMIFnCS[4:2] high (SS = 0)	(WH)*E-3	(WH)*E	(WH)*E+3	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–1], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the EMIF User's guide for more information.
(2) E = EMIF_CLK period in ns.
(3) EWC = external wait cycles determined by EMIFnWAIT input signal. EWC supports the following range of values. EWC[256–1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the EMIF User's Guide for more information.

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Table 4-28. EMIF Asynchronous Memory Switching Characteristics[1][2][3] (continued)

NO	Parameter		Value			Unit
			MIN	NOM	MAX	
		Output hold time, EMIFnWE high to EMIFCS[4:2] high (SS = 1)	-3	0	+3	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMIFBA[1:0] valid to EMIFnWE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, EMIFnWE high to EMIFBA[1:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMIFBA[1:0] valid to EMIFnWE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, EMIFnWE high to EMIFBA[1:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMIFADDR[21:0] valid to EMIFnWE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, EMIFnWE high to EMIFADDR[21:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
24	$t_{w(EMWEL)}$	EMIFnWE active low width (EW = 0)	(WST)*E-3	(WST)*E	(WST)*E+3	ns
		EMIFnWE active low width (EW = 1)	(WST+(EWC*16)) *E-3	(WST+(EWC*16))*E	(WST+(EWC*16)) *E+3	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMIFnWAIT deasserted to EMIFnWE high	3E-3	4E	4E+3	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMIFDATA[15:0] valid to EMIFnWE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, EMIFnWE high to EMIFDATA[15:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns

Table 4-29. EMIF Synchronous Memory Timing Requirements

NO.	Parameter		MIN	MAX	Unit
19	$t_{su(EMIFDV-EM\_CLKH)}$	Input setup time, read data valid on EMIFDATA[15:0] before EMIF_CLK rising	1		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMIFDATA[15:0] after EMIF_CLK rising	1.5		ns

Table 4-30. EMIF Synchronous Memory Switching Characteristics

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMIF_CLK	15		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMIF_CLK high or low	5		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMIF_CLK rising to EMIFnCS[0] valid		7	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMIF_CLK rising to EMIFnCS[0] invalid	1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMIF_CLK rising to EMIFnDQM[1:0] valid		7	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMIF_CLK rising to EMIFnDQM[1:0] invalid	1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMIF_CLK rising to EMIFADDR[21:0] and EMIFBA[1:0] valid		7	ns

Table 4-30. EMIF Synchronous Memory Switching Characteristics (continued)

NO.	Parameter		MIN	MAX	Unit
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMIF_CLK rising to EMIFADDR[21:0] and EMIFBA[1:0] invalid	1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMIF_CLK rising to EMIFDATA[15:0] valid		7	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMIF_CLK rising to EMIFDATA[15:0] invalid	1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMIF_CLK rising to EMIFnRAS valid		7	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMIF_CLK rising to EMIFnRAS invalid	1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMIF_CLK rising to EMIFnCAS valid		7	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMIF_CLK rising to EMIFnCAS invalid	1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMIF_CLK rising to EMIFnWE valid		7	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMIF_CLK rising to EMIFnWE invalid	1		ns
17	$t_{dis(CLKH-DHZ)}$	Delay time, EMIF_CLK rising to EMIFDATA[15:0] tri-stated		7	ns
18	$t_{ena(CLKH-DLZ)}$	Output hold time, EMIF_CLK rising to EMIFDATA[15:0] driving	1		ns

4.15 Vectored Interrupt Manager

The vectored interrupt manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on this device. Interrupts are caused by events outside of the normal flow of program execution. Normally, these events require a timely response from the central processing unit (CPU); therefore, when an interrupt occurs, the CPU switches execution from the normal program flow to an interrupt service routine (ISR).

4.15.1 VIM Features

The VIM module has the following features:

- Supports 96 interrupt channels.
  - Provides programmable priority and enable for interrupt request lines.
- Provides a direct hardware dispatch mechanism for fastest IRQ dispatch.
- Provides two software dispatch mechanisms when the CPU VIC port is not used.
  - Index interrupt
  - Register vectored interrupt
- Parity protected vector interrupt table against soft errors.

4.15.2 Interrupt Request Assignments

Table 4-31. Interrupt Request Assignments

Modules	Interrupt Sources	Default VIM Interrupt Channel
ESM	ESM High level interrupt (NMI)	0
Reserved	Reserved	1
RTI	RTI compare interrupt 0	2
RTI	RTI compare interrupt 1	3
RTI	RTI compare interrupt 2	4
RTI	RTI compare interrupt 3	5
RTI	RTI overflow interrupt 0	6
RTI	RTI overflow interrupt 1	7
RTI	RTI timebase interrupt	8
GIO	GIO interrupt A	9
N2HET1	N2HET1 level 0 interrupt	10
HET TU1	HET TU1 level 0 interrupt	11
MIBSPI1	MIBSPI1 level 0 interrupt	12
LIN	LIN level 0 interrupt	13
MIBADC1	MIBADC1 event group interrupt	14
MIBADC1	MIBADC1 sw group 1 interrupt	15
DCAN1	DCAN1 level 0 interrupt	16
SPI2	SPI2 level 0 interrupt	17
Reserved	Reserved	18
CRC	CRC Interrupt	19
ESM	ESM Low level interrupt	20
SYSTEM	Software interrupt (SSI)	21
CPU	PMU Interrupt	22
GIO	GIO interrupt B	23
N2HET1	N2HET1 level 1 interrupt	24
HET TU	HET TU level 1 interrupt	25
MIBSPI	MIBSPI level 1 interrupt	26

Table 4-31. Interrupt Request Assignments (continued)

Modules	Interrupt Sources	Default VIM Interrupt Channel
LIN	LIN level 1 interrupt	27
MIBADC	MIBADC sw group 2 interrupt	28
DCAN1	DCAN1 level 1 interrupt	29
SPI2	SPI2 level 1 interrupt	30
MIBADC1	MIBADC1 magnitude compare interrupt	31
Reserved	Reserved	32
DMA	FTCA interrupt	33
DMA	LFSA interrupt	34
DCAN2	DCAN2 level 0 interrupt	35
DMM	DMM level 0 interrupt	36
MIBSPI3	MIBSPI3 level 0 interrupt	37
MIBSPI3	MIBSPI3 level 1 interrupt	38
DMA	HBCA interrupt	39
DMA	BTCA interrupt	40
EMIF	AEMIFINT3	41
DCAN2	DCAN2 level 1 interrupt	42
DMM	DMM level 1 interrupt	43
DCAN1	DCAN1 IF3 interrupt	44
DCAN3	DCAN3 level 0 interrupt	45
DCAN2	DCAN2 IF3 interrupt	46
FPU	FPU interrupt	47
Reserved	Reserved	48
SPI4	SPI4 level 0 interrupt	49
MIBADC2	MibADC2 event group interrupt	50
MIBADC2	MibADC2 sw group1 interrupt	51
Reserved	Reserved	52
MIBSPI5	MIBSPI5 level 0 interrupt	53
SPI4	SPI4 level 1 interrupt	54
DCAN3	DCAN3 level 1 interrupt	55
MIBSPI5	MIBSPI5 level 1 interrupt	56
MIBADC2	MibADC2 sw group2 interrupt	57
Reserved	Reserved	58
MIBADC2	MibADC2 magnitude compare interrupt	59
DCAN3	DCAN3 IF3 interrupt	60
FMC	FSM_DONE interrupt	61
Reserved	Reserved	62
N2HET2	N2HET2 level 0 interrupt	63
SCI	SCI level 0 interrupt	64
HET TU2	HET TU2 level 0 interrupt	65
I2C	I2C level 0 interrupt	66
Reserved	Reserved	67-72
N2HET2	N2HET2 level 1 interrupt	73
SCI	SCI level 1 interrupt	74
HET TU2	HET TU2 level 1 interrupt	75
Ethernet	C0_MISC_PULSE	76
Ethernet	C0_TX_PULSE	77
Ethernet	C0_THRESH_PULSE	78

Table 4-31. Interrupt Request Assignments (continued)

Modules	Interrupt Sources	Default VIM Interrupt Channel
Ethernet	C0_RX_PULSE	79
HWAG1	HWA_INT_REQ_H	80
HWAG2	HWA_INT_REQ_H	81
DCC1	DCC done interrupt	82
Reserved	Reserved	84-87
HWAG1	HWA_INT_REQ_L	88
HWAG2	HWA_INT_REQ_L	89
Reserved	Reserved	90-95

NOTE

Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry; therefore only request channels 0..94 can be used and are offset by 1 address in the VIM RAM.

NOTE

The lower-order interrupt channels are higher priority channels than the higher-order interrupt channels.

NOTE

The application can change the mapping of interrupt sources to the interrupt channels via the interrupt channel control registers (CHANCTRLx) inside the VIM module.

4.16 DMA Controller

The DMA controller is used to transfer data between two locations in the memory map in the background of CPU operations. Typically, the DMA is used to:

- Transfer blocks of data between external and internal data memories
- Restructure portions of internal data memory
- Continually service a peripheral

4.16.1 DMA Features

- CPU independent data transfer
- One master port - PortB (64 bits wide) that interfaces to the RM4x Memory System.
- FIFO buffer(4 entries deep and each 64bit wide)
- Channel control information is stored in RAM protected by parity
- 16 channels with individual enable
- Channel chaining capability
- 32 peripheral DMA requests
- Hardware and Software DMA requests
- 8, 16, 32 or 64-bit transactions supported
- Multiple addressing modes for source/destination (fixed, increment, offset)
- Auto-initiation
- Power-management mode
- Memory Protection with four configurable memory regions

4.16.2 Default DMA Request Map

The DMA module on this microcontroller has 16 channels and up to 32 hardware DMA requests. The module contains DREQASIx registers which are used to map the DMA requests to the DMA channels. By default, channel 0 is mapped to request 0, channel 1 to request 1, and so on.

Some DMA requests have multiple sources, as shown in Table 4-32. The application must ensure that only one of these DMA request sources is enabled at any time.

Table 4-32. DMA Request Line Connection

Modules	DMA Request Sources	DMA Request
MIBSPI1	MIBSPI1[1](1)	DMAREQ[0]
MIBSPI1	MIBSPI1[0](2)	DMAREQ[1]
SPI2	SPI2 receive	DMAREQ[2]
SPI2	SPI2 transmit	DMAREQ[3]
MIBSPI1 / MIBSPI3 / DCAN2	MIBSPI1[2] / MIBSPI3[2] / DCAN2 IF3	DMAREQ[4]
MIBSPI1 / MIBSPI3 / DCAN2	MIBSPI1[3] / MIBSPI3[3] / DCAN2 IF2	DMAREQ[5]
DCAN1 / MIBSPI5	DCAN1 IF2 / MIBSPI5[2]	DMAREQ[6]
MIBADC1 / MIBSPI5	MIBADC1 event / MIBSPI5[3]	DMAREQ[7]
MIBSPI1 / MIBSPI3 / DCAN1	MIBSPI1[4] / MIBSPI3[4] / DCAN1 IF1	DMAREQ[8]
MIBSPI1 / MIBSPI3 / DCAN2	MIBSPI1[5] / MIBSPI3[5] / DCAN2 IF1	DMAREQ[9]
MIBADC1 / I2C / MIBSPI5	MIBADC1 G1 / I2C receive / MIBSPI5[4]	DMAREQ[10]
MIBADC1 / I2C / MIBSPI5	MIBADC1 G2 / I2C transmit / MIBSPI5[5]	DMAREQ[11]
RTI / MIBSPI1 / MIBSPI3	RTI DMAREQ0 / MIBSPI1[6] / MIBSPI3[6]	DMAREQ[12]
RTI / MIBSPI1 / MIBSPI3	RTI DMAREQ1 / MIBSPI1[7] / MIBSPI3[7]	DMAREQ[13]
MIBSPI3 / MibADC2 / MIBSPI5	MIBSPI3[1](1) / MibADC2 event / MIBSPI5[6]	DMAREQ[14]
MIBSPI3 / MIBSPI5	MIBSPI3[0](2) / MIBSPI5[7]	DMAREQ[15]
MIBSPI1 / MIBSPI3 / DCAN1 / MibADC2	MIBSPI1[8] / MIBSPI3[8] / DCAN1 IF3 / MibADC2 G1	DMAREQ[16]
MIBSPI1 / MIBSPI3 / DCAN3 / MibADC2	MIBSPI1[9] / MIBSPI3[9] / DCAN3 IF1 / MibADC2 G2	DMAREQ[17]
RTI / MIBSPI5	RTI DMAREQ2 / MIBSPI5[8]	DMAREQ[18]
RTI / MIBSPI5	RTI DMAREQ3 / MIBSPI5[9]	DMAREQ[19]
N2HET1 / N2HET2 / DCAN3	N2HET1 DMAREQ[4] / N2HET2 DMAREQ[4] / DCAN3 IF2	DMAREQ[20]
N2HET1 / N2HET2 / DCAN3	N2HET1 DMAREQ[5] / N2HET2 DMAREQ[5] / DCAN3 IF3	DMAREQ[21]
MIBSPI1 / MIBSPI3 / MIBSPI5	MIBSPI1[10] / MIBSPI3[10] / MIBSPI5[10]	DMAREQ[22]
MIBSPI1 / MIBSPI3 / MIBSPI5	MIBSPI1[11] / MIBSPI3[11] / MIBSPI5[11]	DMAREQ[23]
N2HET1 / N2HET2 / SPI4 / MIBSPI5	N2HET1 DMAREQ[6] / N2HET2 DMAREQ[6] / SPI4 receive / MIBSPI5[12]	DMAREQ[24]
N2HET1 / N2HET2 / SPI4 / MIBSPI5	N2HET1 DMAREQ[7] / N2HET2 DMAREQ[7] / SPI4 transmit / MIBSPI5[13]	DMAREQ[25]
CRC / MIBSPI1 / MIBSPI3	CRC DMAREQ[0] / MIBSPI1[12] / MIBSPI3[12]	DMAREQ[26]
CRC / MIBSPI1 / MIBSPI3	CRC DMAREQ[1] / MIBSPI1[13] / MIBSPI3[13]	DMAREQ[27]
LIN / MIBSPI5	LIN receive / MIBSPI5[14]	DMAREQ[28]
LIN / MIBSPI5	LIN transmit / MIBSPI5[15]	DMAREQ[29]
MIBSPI1 / MIBSPI3 / SCI / MIBSPI5	MIBSPI1[14] / MIBSPI3[14] / SCI receive / MIBSPI5[1](1)	DMAREQ[30]
MIBSPI1 / MIBSPI3 / SCI / MIBSPI5	MIBSPI1[15] / MIBSPI3[15] / SCI transmit / MIBSPI5[0](2)	DMAREQ[31]

(1) SPI1, SPI3, SPI5 receive in mode
(2) SPI1, SPI3, SPI5 transmit in mode

4.17 Real Time Interrupt Module

The real-time interrupt (RTI) module provides timer functionality for operating systems and for benchmarking code. The RTI module can incorporate several counters that define the timebases needed for scheduling an operating system.

The timers also allow you to benchmark certain areas of code by reading the values of the counters at the beginning and the end of the desired code range and calculating the difference between the values.

4.17.1 Features

The RTI module has the following features:

- Two independent 64 bit counter blocks
- Four configurable compares for generating operating system ticks or DMA requests. Each event can be driven by either counter block 0 or counter block 1.
- Fast enabling/disabling of events
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block

4.17.2 Block Diagrams

Figure 4-17 shows a high-level block diagram for one of the two 64-bit counter blocks inside the RTI module. Both the counter blocks are identical except the Network Time Unit (NTUx) inputs are only available as time base inputs for the counter block 0.

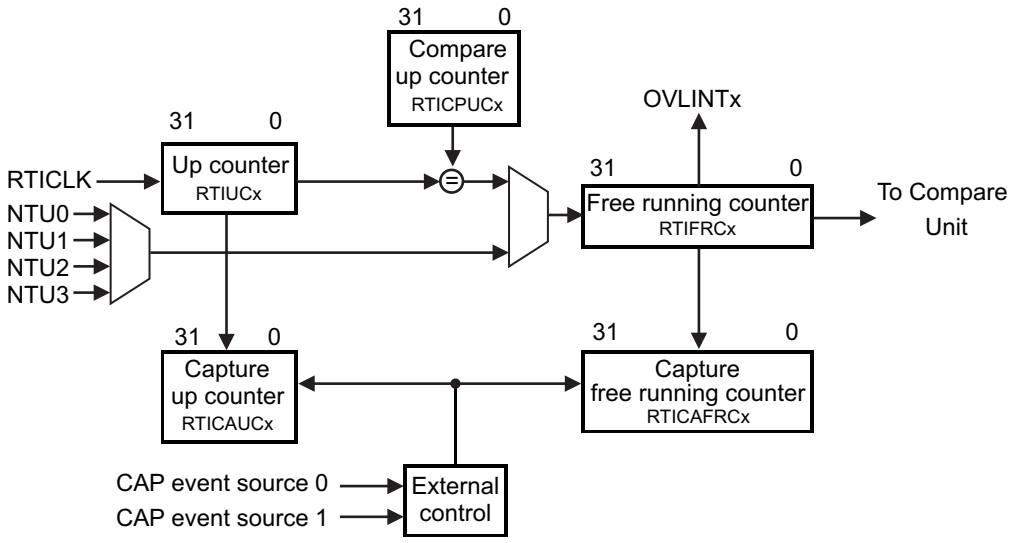

Figure 4-17. Counter Block Diagram

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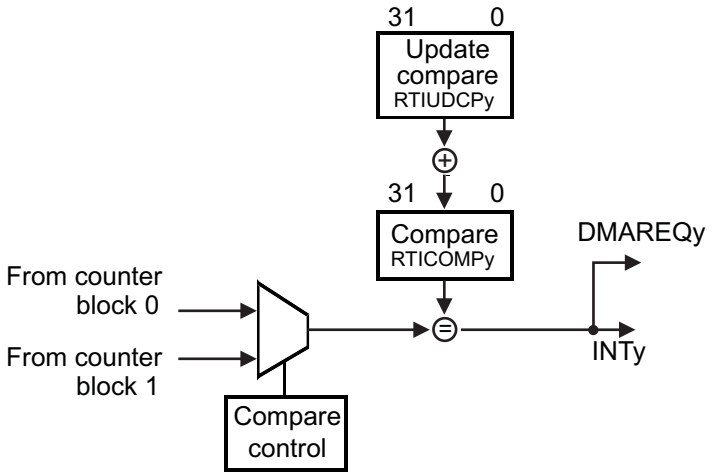

Figure 4-18. Compare Block Diagram

4.17.3 Clock Source Options

The RTI module uses the RTI1CLK clock domain for generating the RTI time bases.

The application can select the clock source for the RTI1CLK by configuring the RCLKSRC register in the System module at address 0xFFFFFF50. The default source for RTI1CLK is VCLK.

For more information on clock sources refer to Table 4-8 and Table 4-13.

4.17.4 Network Time Synchronization Inputs

The RTI module supports 4 Network Time Unit (NTU) inputs that signal internal system events, and which can be used to synchronize the time base used by the RTI module. On this device, these NTU inputs are connected as shown below.

Table 4-33. Network Time Synchronization Inputs

NTU Input	Source
0	Reserved
1	Reserved
2	PLL2 Clock output
3	EXTCLKIN1 clock input

4.18 Error Signaling Module

The Error Signaling Module (ESM) manages the various error conditions on the RM4x microcontroller. The error condition is handled based on a fixed severity level assigned to it. Any severe error condition can be configured to drive a low level on a dedicated device terminal called nERROR. This can be used as an indicator to an external monitor circuit to put the system into a safe state.

4.18.1 Features

The features of the Error Signaling Module are:

- 128 interrupt/error channels are supported, divided into 3 different groups
  - 64 channels with maskable interrupt and configurable error pin behavior
  - 32 error channels with non-maskable interrupt and predefined error pin behavior
  - 32 channels with predefined error pin behavior only
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability

4.18.2 ESM Channel Assignments

The Error Signaling Module (ESM) integrates all the device error conditions and groups them in the order of severity. Group1 is used for errors of the lowest severity while Group3 is used for errors of the highest severity. The device response to each error is determined by the severity group it is connected to. Table 4-35 shows the channel assignment for each group.

Table 4-34. ESM Groups

ERROR GROUP	INTERRUPT CHARACTERISTICS	INFLUENCE ON ERROR PIN
Group1	maskable, low or high priority	configurable
Group2	non-maskable, high priority	fixed
Group3	no interrupt generated	fixed

Table 4-35. ESM Channel Assignments

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group1	0
MibADC2 - parity	Group1	1
DMA - MPU	Group1	2
DMA - parity	Group1	3
Reserved	Group1	4
DMA - imprecise read error	Group1	5
FMC - correctable error: bus1 and bus2 interfaces (does not include accesses to EEPROM bank)	Group1	6
N2HET1/N2HET2 - parity	Group1	7
HET TU1/HET TU2 - parity	Group1	8
HET TU1/HET TU2 - MPU	Group1	9
PLL - Slip	Group1	10
Clock Monitor - interrupt	Group1	11
Reserved	Group1	12
DMA - imprecise write error	Group1	13
Reserved	Group1	14
VIM RAM - parity	Group1	15
Reserved	Group1	16
MibSPI1 - parity	Group1	17

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Table 4-35. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
MibSPI3 - parity	Group1	18
MibADC1 - parity	Group1	19
Reserved	Group1	20
DCAN1 - parity	Group1	21
DCAN3 - parity	Group1	22
DCAN2 - parity	Group1	23
MibSPI5 - parity	Group1	24
Reserved	Group1	25
RAM even bank (B0TCM) - correctable error	Group1	26
CPU - selftest	Group1	27
RAM odd bank (B1TCM) - correctable error	Group1	28
Reserved	Group1	29
DCC1 - error	Group1	30
CCM-R4 - selftest	Group1	31
Reserved	Group1	32
Reserved	Group1	33
Reserved	Group1	34
FMC - correctable error (EEPROM bank access)	Group1	35
FMC - uncorrectable error (EEPROM bank access)	Group1	36
IOMM - Mux configuration error	Group1	37
Power domain controller compare error	Group1	38
Power domain controller self-test error	Group1	39
eFuse Controller Error – this error signal is generated when any bit in the eFuse controller error status register is set. The application can choose to generate an interrupt whenever this bit is set to service any eFuse controller error conditions.	Group1	40
eFuse Controller - Self Test Error. This error signal is generated only when a self test on the eFuse controller generates an error condition. When this error signal is set, group 1 channel 40 error signal will also be set.	Group1	41
PLL2 - Slip	Group1	42
Ethernet Controller master interface	Group1	43
Reserved	Group1	44
Reserved	Group1	45
Reserved	Group1	46
Reserved	Group1	47
Reserved	Group1	48
Reserved	Group1	49
Reserved	Group1	50
Reserved	Group1	51
Reserved	Group1	52
Reserved	Group1	53
Reserved	Group1	54
Reserved	Group1	55
Reserved	Group1	56
Reserved	Group1	57
Reserved	Group1	58
Reserved	Group1	59
Reserved	Group1	60
Reserved	Group1	61

Table 4-35. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
DCC2 - error	Group1	62
Reserved	Group1	63
Reserved	Group2	0
Reserved	Group2	1
CCMR4 - compare	Group2	2
Reserved	Group2	3
FMC - uncorrectable error (address parity on bus1 accesses)	Group2	4
Reserved	Group2	5
RAM even bank (B0TCM) - uncorrectable error	Group2	6
Reserved	Group2	7
RAM odd bank (B1TCM) - uncorrectable error	Group2	8
Reserved	Group2	9
RAM even bank (B0TCM) - address bus parity error	Group2	10
Reserved	Group2	11
RAM odd bank (B1TCM) - address bus parity error	Group2	12
Reserved	Group2	13
Reserved	Group2	14
Reserved	Group2	15
Flash (ATCM) - ECC live lock detect	Group2	16
Reserved	Group2	17
Reserved	Group2	18
Reserved	Group2	19
Reserved	Group2	20
Reserved	Group2	21
Reserved	Group2	22
Reserved	Group2	23
RTI_WWD_NMI	Group2	24
Reserved	Group2	25
Reserved	Group2	26
Reserved	Group2	27
Reserved	Group2	28
Reserved	Group2	29
Reserved	Group2	30
Reserved	Group2	31
Reserved	Group3	0
eFuse Controller - autoload error	Group3	1
Reserved	Group3	2
RAM even bank (B0TCM) - ECC uncorrectable error	Group3	3
Reserved	Group3	4
RAM odd bank (B1TCM) - ECC uncorrectable error	Group3	5
Reserved	Group3	6
FMC - uncorrectable error: bus1 and bus2 interfaces (does not include address parity error and errors on accesses to EEPROM bank)	Group3	7
Reserved	Group3	8
Reserved	Group3	9
Reserved	Group3	10
Reserved	Group3	11

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Table 4-35. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group3	12
Reserved	Group3	13
Reserved	Group3	14
Reserved	Group3	15
Reserved	Group3	16
Reserved	Group3	17
Reserved	Group3	18
Reserved	Group3	19
Reserved	Group3	20
Reserved	Group3	21
Reserved	Group3	22
Reserved	Group3	23
Reserved	Group3	24
Reserved	Group3	25
Reserved	Group3	26
Reserved	Group3	27
Reserved	Group3	28
Reserved	Group3	29
Reserved	Group3	30
Reserved	Group3	31

4.19 Reset / Abort / Error Sources

Table 4-36. Reset/Abort/Error Sources

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP group.channel
CPU TRANSACTIONS			
Precise write error (NCNB/Strongly Ordered)	User/Privilege	Precise Abort (CPU)	n/a
Precise read error (NCB/Device or Normal)	User/Privilege	Precise Abort (CPU)	n/a
Imprecise write error (NCB/Device or Normal)	User/Privilege	Imprecise Abort (CPU)	n/a
Illegal instruction	User/Privilege	Undefined Instruction Trap (CPU)(1)	n/a
MPU access violation	User/Privilege	Abort (CPU)	n/a
SRAM			
B0 TCM (even) ECC single error (correctable)	User/Privilege	ESM	1.26
B0 TCM (even) ECC double error (non-correctable)	User/Privilege	Abort (CPU), ESM => nERROR	3.3
B0 TCM (even) uncorrectable error (i.e. redundant address decode)	User/Privilege	ESM => NMI	2.6
B0 TCM (even) address bus parity error	User/Privilege	ESM => NMI	2.10
B1 TCM (odd) ECC single error (correctable)	User/Privilege	ESM	1.28
B1 TCM (odd) ECC double error (non-correctable)	User/Privilege	Abort (CPU), ESM => nERROR	3.5
B1 TCM (odd) uncorrectable error (i.e. redundant address decode)	User/Privilege	ESM => NMI	2.8
B1 TCM (odd) address bus parity error	User/Privilege	ESM => NMI	2.12
FLASH			
FMC correctable error - Bus1 and Bus2 interfaces	User/Privilege	ESM	1.6
FMC uncorrectable error - Bus1 accesses (does not include address parity error)	User/Privilege	Abort (CPU), ESM => nERROR	3.7
FMC uncorrectable error - Bus2 accesses (does not include address parity error and EEPROM bank accesses)	User/Privilege	ESM => nERROR	3.7
FMC uncorrectable error - address parity error on Bus1 accesses	User/Privilege	ESM => NMI	2.4
FMC correctable error - Accesses to EEPROM bank	User/Privilege	ESM	1.35
FMC uncorrectable error - Accesses to EEPROM bank	User/Privilege	ESM	1.36
DMA TRANSACTIONS			
External imprecise error on read (Illegal transaction with ok response)	User/Privilege	ESM	1.5
External imprecise error on write (Illegal transaction with ok response)	User/Privilege	ESM	1.13
Memory access permission violation	User/Privilege	ESM	1.2
Memory parity error	User/Privilege	ESM	1.3
DMM TRANSACTIONS			
External imprecise error on read (Illegal transaction with ok response)	User/Privilege	ESM	1.5
External imprecise error on write (Illegal transaction with ok response)	User/Privilege	ESM	1.13
HET TU (HTU)			
NCNB (Strongly Ordered) transaction with slave error response	User/Privilege	Interrupt => VIM	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	Interrupt => VIM	n/a
Memory access permission violation	User/Privilege	ESM	1.9

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the instruction reaches the execute stage of the CPU.

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Table 4-36. Reset/Abort/Error Sources (continued)

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP group.channel
Memory parity error	User/Privilege	ESM	1.8
HET TU2 (HTU2)			
NCNB (Strongly Ordered) transaction with slave error response	User/Privilege	Interrupt => VIM	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	Interrupt => VIM	n/a
Memory access permission violation	User/Privilege	ESM	1.9
Memory parity error	User/Privilege	ESM	1.8
N2HET			
Memory parity error	User/Privilege	ESM	1.7
N2HET2			
Memory parity error	User/Privilege	ESM	1.7
ETHERNET MASTER INTERFACE			
Any error reported by slave being accessed	User/Privilege	ESM	1.43
MIBSPI			
MibSPI1 memory parity error	User/Privilege	ESM	1.17
MibSPI3 memory parity error	User/Privilege	ESM	1.18
MibSPI5 memory parity error	User/Privilege	ESM	1.24
MIBADC			
MibADC Memory parity error	User/Privilege	ESM	1.19
MibADC2 Memory parity error	User/Privilege	ESM	1.1
DCAN			
DCAN1 memory parity error	User/Privilege	ESM	1.21
DCAN2 memory parity error	User/Privilege	ESM	1.23
DCAN3 memory parity error	User/Privilege	ESM	1.22
PLL			
PLL slip error	User/Privilege	ESM	1.10
PLL #2 slip error	User/Privilege	ESM	1.42
CLOCK MONITOR			
Clock monitor interrupt	User/Privilege	ESM	1.11
DCC			
DCC1 error	User/Privilege	ESM	1.30
DCC2 error	User/Privilege	ESM	1.62
CCM-R4			
Self test failure	User/Privilege	ESM	1.31
Compare failure	User/Privilege	ESM => NMI	2.2
VIM			
Memory parity error	User/Privilege	ESM	1.15
VOLTAGE MONITOR			
VMON out of voltage range	n/a	Reset	n/a
CPU SELFTEST (LBIST)			
CPU Selftest (LBIST) error	User/Privilege	ESM	1.27
PIN MULTIPLEXING CONTROL			
Mux configuration error	User/Privilege	ESM	1.37
POWER DOMAIN CONTROL			
PSCON compare error	User/Privilege	ESM	1.38
PSCON self-test error	User/Privilege	ESM	1.39
eFuse Controller			
eFuse Controller error	User/Privilege	ESM	3.1

Table 4-36. Reset/Abort/Error Sources (continued)

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP group.channel
eFuse Controller - Any bit set in the error status register	User/Privilege	ESM	1.40
eFuse Controller self-test error	User/Privilege	ESM	1.41
WINDOWED WATCHDOG			
WWD Non-Maskable Interrupt exception	n/a	ESM	2.24
ERRORS REFLECTED IN THE SYSESR REGISTER			
Power-Up Reset	n/a	Reset	n/a
Oscillator fail / PLL slip(2)	n/a	Reset	n/a
Watchdog exception	n/a	Reset	n/a
CPU Reset (driven by the CPU STC)	n/a	Reset	n/a
Software Reset	n/a	Reset	n/a
External Reset	n/a	Reset	n/a

(2) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

4.20 Digital Windowed Watchdog

This device includes a digital windowed watchdog (DWWD) module that protects against runaway code execution.

The DWWD module allows the application to configure the time window within which the DWWD module expects the application to service the watchdog. A watchdog violation occurs if the application services the watchdog outside of this window, or fails to service the watchdog at all. The application can choose to generate a system reset or a non-maskable interrupt to the CPU in case of a watchdog violation.

The watchdog is disabled by default and must be enabled by the application. Once enabled, the watchdog can only be disabled upon a system reset.

4.21 Debug Subsystem

4.21.1 Block Diagram

The device contains an ICEPICK module to allow JTAG access to the scan chains.

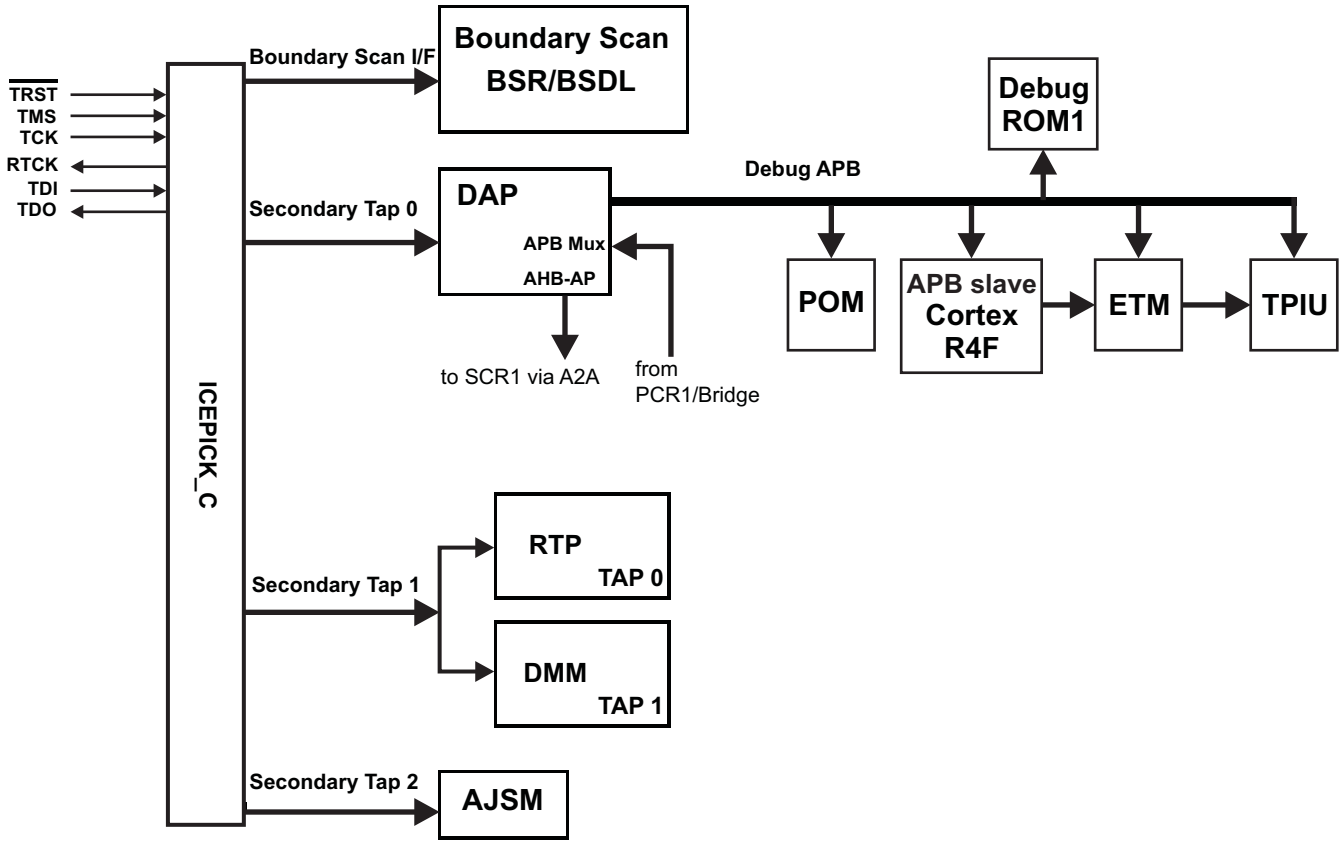

Figure 4-19. ZWT Debug Subsystem Block Diagram

4.21.2 Debug Components Memory Map

Table 4-37. Debug Components Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4F Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect
ETM-R4	CSCS2	0xFFA0_2000	0xFFA0_2FFF	4KB	4KB	Reads return zeros, writes have no effect
CoreSight TPIU	CSCS3	0xFFA0_3000	0xFFA0_3FFF	4KB	4KB	Reads return zeros, writes have no effect

4.21.3 JTAG Identification Code

The JTAG ID code for this device is 0x0D8A002F. This is the same as the device ICEPick Identification Code.

4.21.4 Debug ROM

The Debug ROM stores the location of the components on the Debug APB bus:

Table 4-38. Debug ROM table

ADDRESS	DESCRIPTION	VALUE
0x000	pointer to Cortex-R4F	0x0000 1003
0x001	ETM-R4	0x0000 2003
0x002	TPIU	0x0000 3003
0x003	POM	0x0000 4003
0x004	end of table	0x0000 0000

4.21.5 JTAG Scan Interface Timings

Table 4-39. JTAG Scan Interface Timing(1)

No.	Parameter		Min	MAX	Unit
	fTCK	TCK frequency (at HCLKmax)		12	MHz
	fRTCK	RTCK frequency (at TCKmax and HCLKmax)	10		MHz
1	td(TCK -RTCK)	Delay time, TCK to RTCK		24	ns
2	tsu(TDI/TMS - RTCKr)	Setup time, TDI, TMS before RTCK rise (RTCKr)	15		ns
3	th(RTCKr -TDI/TMS)	Hold time, TDI, TMS after RTCKr	0		ns
4	th(RTCKr -TDO)	Hold time, TDO after RTCKf	0		ns
5	td(TCKf -TDO)	Delay time, TDO valid after RTCK fall (RTCKf)		10	ns

(1) Timings for TDO are specified for a maximum of 50pF load on TDO

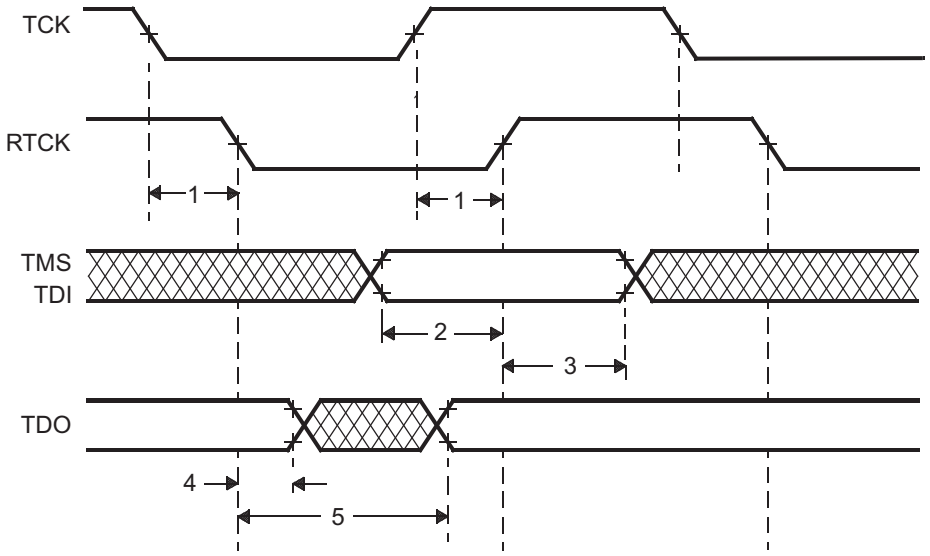

Figure 4-20. JTAG Timing

4.21.6 Advanced JTAG Security Module

This device includes a an Advanced JTAG Security Module (AJSM). which provides maximum security to the device's memory content by allowing users to secure the device after programming.

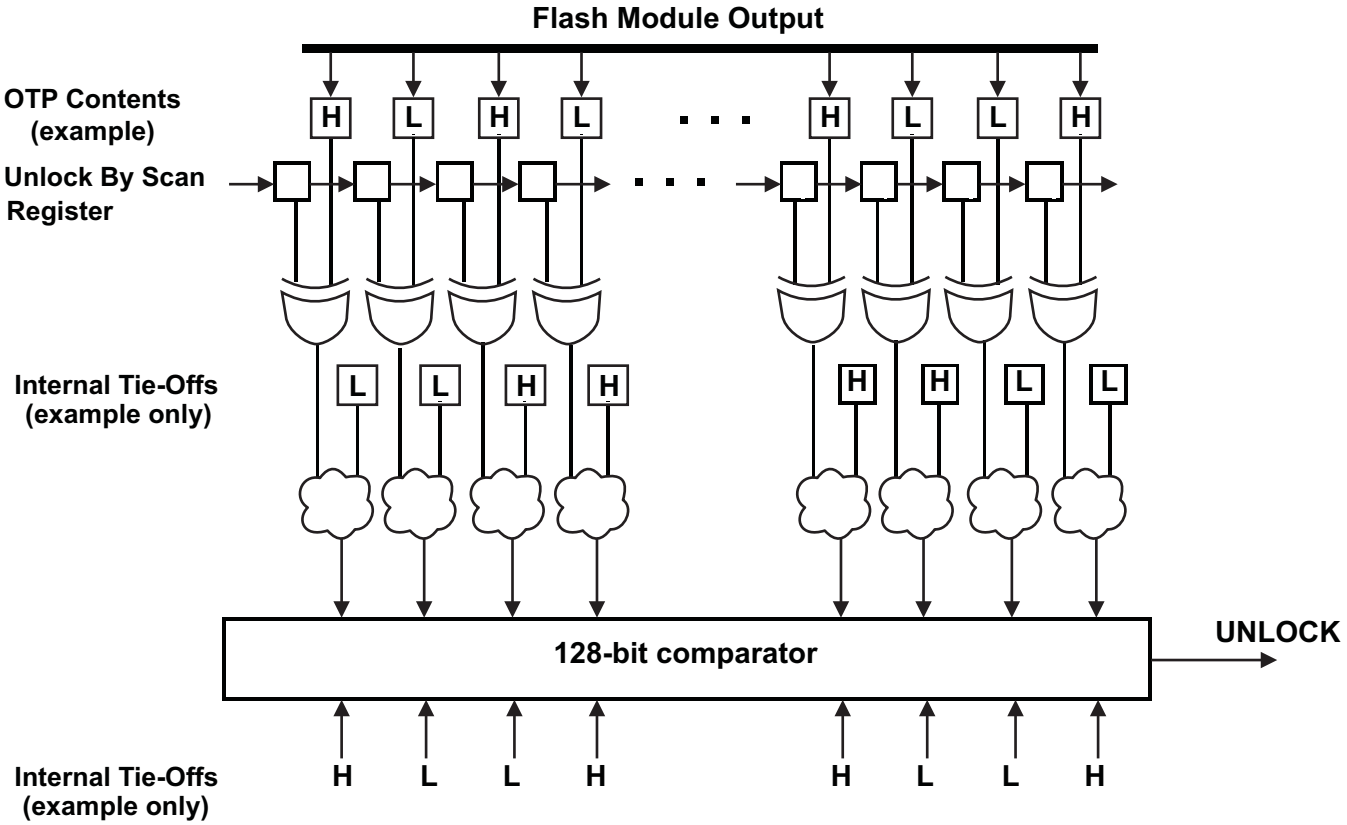

Figure 4-21. AJSM Unlock

The device is unsecure by default by virtue of a 128-bit visible unlock code programmed in the OTP address 0xF0000000.The OTP contents are XOR-ed with the "Unlock By Scan" register contents. The outputs of these XOR gates are again combined with a set of secret internal tie-offs. The output of this combinational logic is compared against a secret hard-wired 128-bit value. A match results in the UNLOCK signal being asserted, so that the device is now unsecure.

A user can secure the device by changing at least one bit in the visible unlock code from 1 to 0. Changing a 0 to 1 is not possible since the visible unlock code is stored in the One Time Programmable (OTP) flash region. Also, changing all the 128 bits to zeros is not a valid condition and will permanently secure the device.

Once secured, a user can unsecure the device by scanning an appropriate value into the "Unlock By Scan" register of the AJSM module. The value to be scanned is such that the XOR of the OTP contents and the Unlock-By-Scan register contents results in the original visible unlock code.

The Unlock-By-Scan register is reset only upon asserting power-on reset (nPORRST).

A secure device only permits JTAG accesses to the AJSM scan chain via the Secondary Tap # 2 of the ICEPick module. All other secondary taps, test taps and the boundary scan interface are not accessible in this state.

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4.21.7 Embedded Trace Macrocell (ETM-R4)

The device contains a ETM-R4 module with a 32-bit internal data port. The ETM-R4 module is connected to a TPIU with a 32-bit data bus; the TPIU provides a 35-bit (32-bit data, 3-bit control) external interface for trace. The ETM-R4 is CoreSight compliant and follows the ETM v3 specification; for more details see ARM CoreSight ETM-R4 TRM specification.

4.21.7.1 ETM TRACECLKIN Selection

The ETM clock source can be selected as either VCLK or the external ETMTRACECLKIN pin. The selection is done by the EXTCTRLOUT[1:0] control bits of the TPIU; the default is '00'. The address of this register is TPIU base address + 0x404.

Before you begin accessing TPIU registers, TPIU should be unlocked via coresight key and 1 or 2 should be written to this register.

Table 4-40. TPIU / TRACECLKIN Selection

EXTCTRLOUT[1:0]	TPIU/TRACECLKIN
00	tied-zero
01	VCLK
10	ETMTRACECLKIN
11	tied-zero

4.21.7.2 Timing Specifications

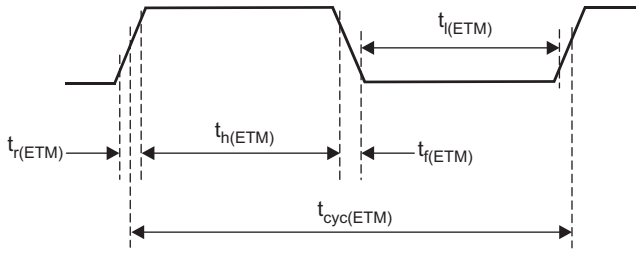

Figure 4-22. ETMTRACECLKOUT Timing

Table 4-41. ETMTRACECLK Timing

Parameter	MIN	Description
$t_{cyc(ETM)}$	$t_{(HCLK)}$ * 4	Clock period
$t_{l(ETM)}$	20ns	Low pulse width
$t_{h(ETM)}$	20ns	High pulse width
$t_{r(ETM)}$	3ns	Clock and data rise time
$t_{f(ETM)}$	3ns	Clock and data fall time

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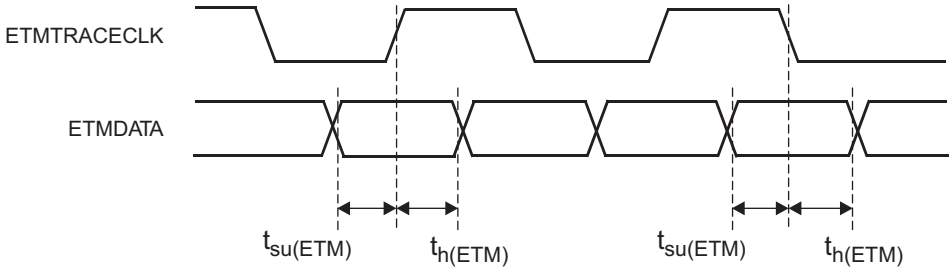

Figure 4-23. ETMDATA Timing

Table 4-42. ETMDATA Timing

Parameter	MIN	Description
$t_{su(ETM)}$	2.5ns	Data setup time
$t_{h(ETM)}$	1.5ns	Data hold time

NOTE

The ETMTRACECLK and ETMDATA timing is based on a 15pF load and for ambient temperature lower than 85°C.

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4.21.8 RAM Trace Port (RTP)

The RTP provides the ability to datalog the RAM contents of the RM4x devices or accesses to peripherals without program intrusion. It can trace all data write or read accesses to internal RAM. In addition, it provides the capability to directly transfer data to a FIFO to support a CPU-controlled transmission of the data. The trace data is transmitted over a dedicated external interface.

4.21.8.1 Features

The RTP offers the following features:

- Two modes of operation - Trace Mode and Direct Data Mode
  - Trace Mode
    - Non-intrusive data trace on write or read operation
    - Visibility of RAM content at any time on external capture hardware
    - Trace of peripheral accesses
    - 2 configurable trace regions for each RAM module to limit amount of data to be traced
    - FIFO to store data and address of data of multiple read/write operations
    - Trace of CPU and/or DMA accesses with indication of the master in the transmitted data packet
  - Direct Data Mode
    - Directly write data with the CPU or trace read operations to a FIFO, without transmitting header and address information
- Dedicated synchronous interface to transmit data to external devices
- Free-running clock generation or clock stop mode between transmissions
- Up to 100 Mbit per sec/pin transfer rate for transmitting data
- Pins not used in functional mode can be used as GIOs

4.21.8.2 Timing Specifications

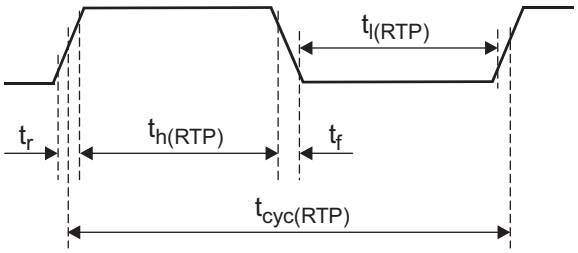

Figure 4-24. RTPCLK Timing

Table 4-43. RTPCLK Timing

Parameter	MIN	Description
$t_{cyc(RTP)}$	$t_{c(HCLK)}$ * 2	Clock period, prescaled from HCLK; must not be faster than HCLK / 2
$t_{h(RTP)}$	$((t_{cyc(RTP)})/2) - ((t_r+t_f)/2)$	High pulse width
$t_{l(RTP)}$	$((t_{cyc(RTP)})/2) - ((t_r+t_f)/2)$	Low pulse width

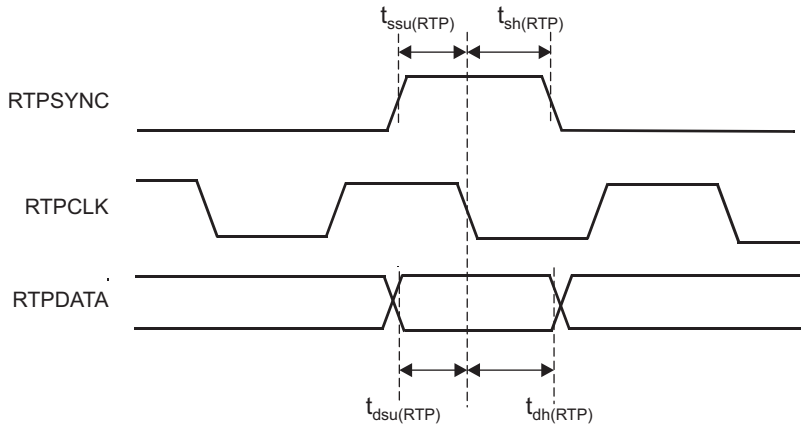

Figure 4-25. RTPDATA Timing

Table 4-44. RTPDATA Timing

Parameter	MIN	Description
$t_{dsu(RTP)}$	3ns	Data setup time
$t_{dh(RTP)}$	2ns	Data hold time
$t_{ssu(RTP)}$	3ns	SYNC setup time
$t_{sh(RTP)}$	2ns	SYNC hold time

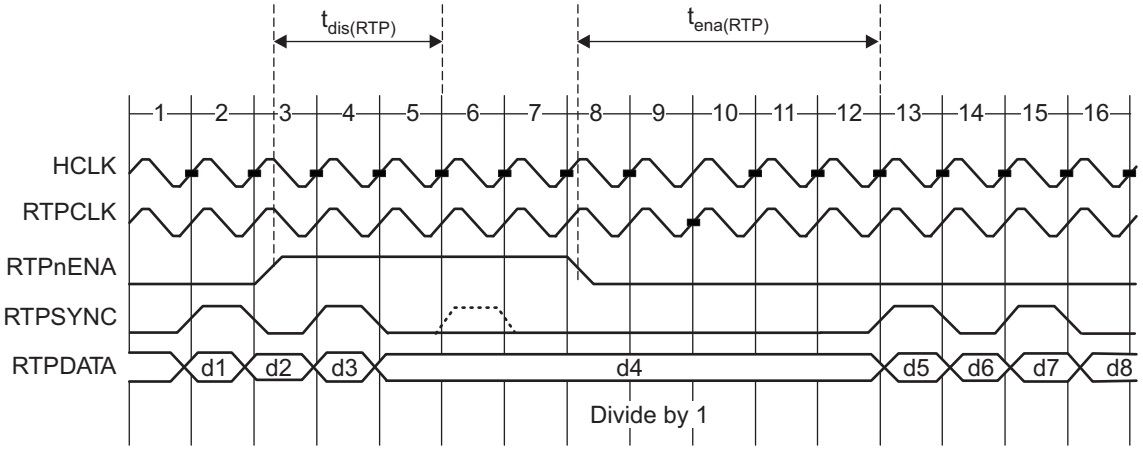

Figure 4-26. RTPnENA timing

Table 4-45. RTPnENA timing

Parameter	MIN	MAX	Description
$t_{dis(RTP)}$	$3t_{c(HCLK)}$ + $t_{r(RTPSYNC)}$ + 12ns		time RTPnENA must go high before what would be the next RTPSYNC, to guarantee delaying the next packet
$t_{ena(RTP)}$	$4t_{c(HCLK)}$ + $t_{r(RTPSYNC)}$	$5t_{c(HCLK)}$ + $t_{r(RTPSYNC)}$ + 12ns	time after RTPnENA goes low before a packet that has been halted, resumes

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4.21.9 Data Modification Module (DMM)

The Data Modification Module (DMM) provides the capability to modify data in the entire 4 GB address space of the RM4x devices from an external peripheral, with minimal interruption of the application.

4.21.9.1 Features

The DMM module has the following features:

- Acts as a bus master, thus enabling direct writes to the 4GB address space without CPU intervention
- Writes to memory locations specified in the received packet (leverages packets defined by trace mode of the RAM trace port (RTP) module
- Writes received data to consecutive addresses, which are specified by the DMM module (leverages packets defined by direct data mode of RTP module)
- Configurable port width (1, 2, 4, 8, 16 pins)
- Up to 100 Mbit/s pin data rate
- Unused pins configurable as GIO pins

4.21.9.2 Timing Specifications

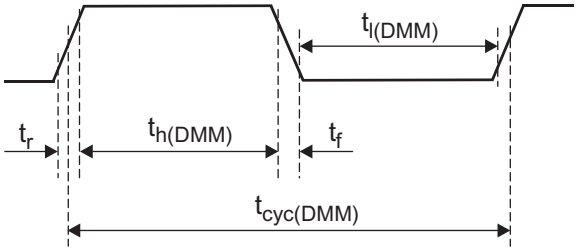

Figure 4-27. DMMCLK Timing

Table 4-46. DMMCLK Timing

Parameter	MIN	Description
$t_{cyc(DMM)}$	$t_{c(HCLK)}$ * 2	Clock period
$t_{h(DMM)}$	(($t_{cyc(DMM)}$)/2) - ((t_r+t_f)/2)	High pulse width
$t_{l(DMM)}$	(($t_{cyc(DMM)}$)/2) - ((t_r+t_f)/2)	Low pulse width

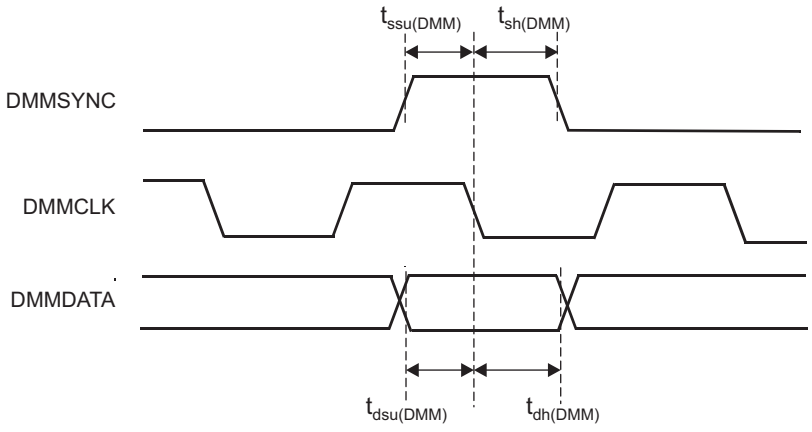

Figure 4-28. DMMDATA Timing

Table 4-47. DMMDATA Timing

Parameter	MIN	Description
$t_{ssu(DMM)}$	2ns	SYNC active to clk falling edge setup time
$t_{sh(DMM)}$	3ns	clk falling edge to SYNC deactive hold time
$t_{dsu(DMM)}$	2ns	DATA to clk falling edge setup time
$t_{dh(DMM)}$	3ns	clk falling edge to DATA hold time

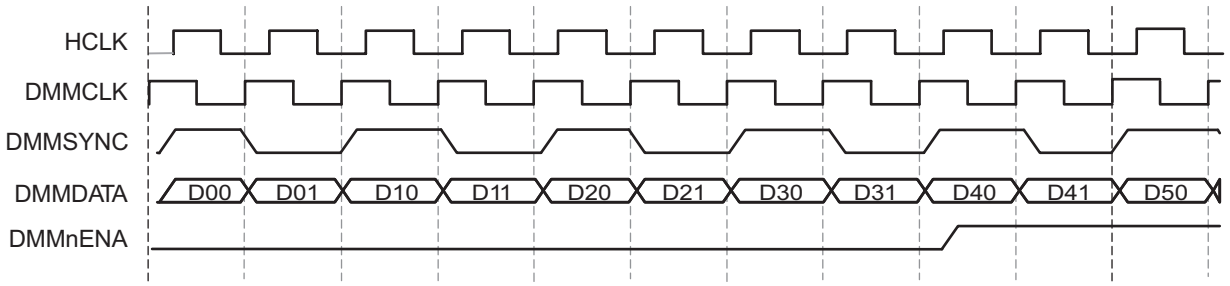

Figure 4-29. DMMnENA Timing

Figure 4-29 shows a case with 1 DMM packet per 2 DMMCLK cycles (Mode = Direct Data Mode, data width = 8, portwidth = 4) where none of the packets received by the DMM are sent out, leading to filling up of the internal buffers. The DMMnENA signal is shown asserted, after the first two packets have been received and synchronised to the HCLK domain. Here, the DMM has the capacity to accept packets D4x, D5x, D6x, D7x. Packet D8 would result in an overflow. Once DMMnENA is asserted, the DMM expects to stop receiving packets after 4 HCLK cycles; once DMMnENA is de-asserted, the DMM can handle packets immediately (after 0 HCLK cycles).

4.21.10 Boundary Scan Chain

The device supports BSDL-compliant boundary scan for testing pin-to-pin compatibility. The boundary scan chain is connected to the Boundary Scan Interface of the ICEPICK module.

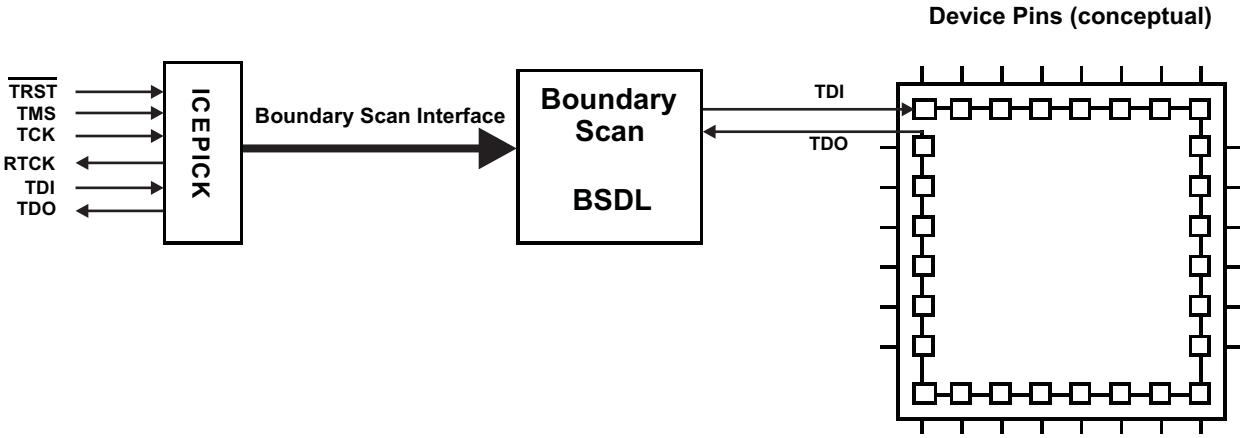

Figure 4-30. Boundary Scan Implementation (Conceptual Diagram)

Data is serially shifted into all boundary-scan buffers via TDI, and out via TDO.

5 Peripheral Information and Electrical Specifications

5.1 Peripheral Legend

Table 5-1. Peripheral Legend

Abbreviation	Full Name
MibADC	Analog To Digital Converter
CCM-R4F	CPU Compare Module - CortexR4F
CRC	Cyclic Redundancy Check
DCAN	Controller Area Network
DCC	Dual Clock Comparator
DMA	Direct Memory Access
DMM	Data Modification Module
EMIF	External Memory Interface
ESM	Error Signaling Module
ETM-R4F	Embedded Trace Macrocell - CortexR4F
GIO	General-Purpose Input/Output
HTU	High End Timer Transfer Unit
I2C	Inter-Integrated Circuit
LIN	Local Interconnect Network
MIBSPI	Multibuffer Serial Peripheral Interface
N2HET	Platform High-End Timer
POM	Parameter Overlay Module
RTI	Real-Time Interrupt Module
RTP	RAM Trace Port
SPI	Serial Peripheral Interface
VIM	Vectored Interrupt Manager

5.2 Multi-Buffered 12bit Analog-to-Digital Converter

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Table 5-2. MibADC Overview

Description	Value
Resolution	12 bits
Monotonic	Assured
Output conversion code	00h to FFFh [00 for $V_{AI} \le AD_{REFLO}$; FFF for $V_{AI} \ge AD_{REFHI}$]

5.2.1 Features

- 10-/12-bit resolution
- AD_{REFHI} and AD_{REFLO} pins (high and low reference voltages)
- Total Sample/Hold/Convert time: 600ns Typical Minimum at 30MHz ADCLK
- One memory region per conversion group is available (event, group 1, group 2)
- Allocation of channels to conversion groups is completely programmable
- Memory regions are serviced either by interrupt or by DMA
- Programmable interrupt threshold counter is available for each group
- Programmable magnitude threshold interrupt for each group for any one channel

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- Option to read either 8-bit, 10-bit or 12-bit values from memory regions
- Single or continuous conversion modes
- Embedded self-test
- Embedded calibration logic
- Enhanced power-down mode
  - Optional feature to automatically power down ADC core when no conversion is in progress
- External event pin (ADEVT) programmable as general-purpose I/O

5.2.2 Event Trigger Options

The ADC module supports 3 conversion groups: Event Group, Group1 and Group2. Each of these 3 groups can be configured to be hardware event-triggered. In that case, the application can select from among 8 event sources to be the trigger for a group's conversions.

5.2.2.1 Default MIBADC Event Trigger Hookup

Table 5-3. MIBADC Event Trigger Hookup

Event #	Source Select Bits For G1, G2 Or Event (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0])	Trigger
1	000	ADEVT
2	001	HET[8]
3	010	HET[10]
4	011	RTI compare 0 interrupt
5	100	HET[12]
6	101	HET[14]
7	110	GIOB[0]
8	111	GIOB[1]

NOTE

For ADEVT, HET and GIOB trigger sources, the connection to the MibADC1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad, or by driving the function from an external trigger source as input.

NOTE

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

5.2.2.2 Alternate MIBADC2 Event Trigger Hookup

Table 5-4. Alternate MIBADC2 Event Trigger Hookup

Event #	Source Select Bits for G1, G2 or Event (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0])	Trigger
1	000	AD2EVT
2	001	N2HET2[5]
3	010	N2HET1[27]
4	011	RTI compare 0
5	100	N2HET1[17]
6	101	N2HET1[19]
7	110	N2HET1[11]

Table 5-4. Alternate MIBADC2 Event Trigger Hookup (continued)

Event #	Source Select Bits for G1, G2 or Event (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0])	Trigger
8	111	N2HET2[13]

The selection between the default MIBADC2 event trigger hook-up versus the alternate event trigger hook-up is done by multiplexing control module register 30 bits 0 and 1.

If 30[0] = 1, then the default MibADC2 event trigger hook-up is used.

If 30[0] = 0 and 30[1] = 1, then the alternate MibADC2 event trigger hook-up is used.

NOTE

For AD2EVT trigger source, the connection to the MibADC2 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring AD2EVT as an output function on to the pad (via the mux control), or by driving the AD2EVT signal from an external trigger source as input. If the mux control module is used to select different functionality instead of the AD2EVT signal, then care must be taken to disable AD2EVT from triggering conversions; there is no multiplexing on the input connections.

NOTE

For N2HETx trigger sources, the connection to the MibADC2 module trigger input is made from the input side of the output buffer (at the N2HETx module boundary). This way, a trigger condition can be generated even if the N2HETx signal is not selected to be output on the pad.

NOTE

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

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5.2.3 ADC Electrical and Timing Specifications

Table 5-5. MibADC Recommended Operating Conditions

Parameter		MIN	MAX	Unit
AD_{REFHI}	A-to-D high-voltage reference source	AD_{REFLO}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	AD_{REFHI}	V
V_{AI}	Analog input voltage	AD_{REFLO}	AD_{REFHI}	V
I_{AIC}	Analog input clamp current (VAI < VSSAD – 0.3 or VAI > VCCAD + 0.3)	- 2	2	mA

Table 5-6. MibADC Electrical Characteristics Over Full Ranges of Recommended Operating Conditions(1)

Parameter		Description/Conditions		MIN	Type	MAX	Unit
R_{mux}	Analog input mux on-resistance	See Figure 5-1				250	Ω
R_{samp}	ADC sample switch on-resistance	See Figure 5-1				250	Ω
C_{mux}	Input mux capacitance	See Figure 5-1				16	pF
C_{samp}	ADC sample capacitance	See Figure 5-1				13	pF
I_{AIL}	Analog off-state input leakage current, for V_{CCAD} = 3.6V maximum	Off-state input leakage per ADC input pin	$V_{SSAD} < V_{IN} < V_{SSAD}$ + 100mV			300	nA
			V_{SSAD} + 100mV < V_{IN} < V_{CCAD} - 200mV			200	nA
			V_{CCAD} - 200mV < V_{IN} < V_{CCAD}			500	nA
I_{AIL}	Analog off-state input leakage current, for V_{CCAD} = 5.5V maximum	Off-state input leakage per ADC input pin	$V_{IN} > V_{SSAD}$, $V_{IN} < V_{SSAD}$ + 300mV			1	µA
			$V_{IN} > V_{SSAD}$ + 300mV, $V_{IN} < V_{CCAD}$ - 300mV			250	nA
			$V_{IN} > V_{CCAD}$ - 300mV, $V_{IN} < V_{CCAD}$			1	µA
$I_{ADREFHI}$	AD_{REFHI} input current	$AD_{REFHI} = V_{CCAD}$, $AD_{REFLO} = V_{SSAD}$				3	mA
I_{CCAD}	Static supply current	Normal operating mode				15	mA
		ADC core in power down mode				5	µA

(1) 1 LSB = (AD_{REFHI} – AD_{REFLO})/ 2^{12} for the MibADC

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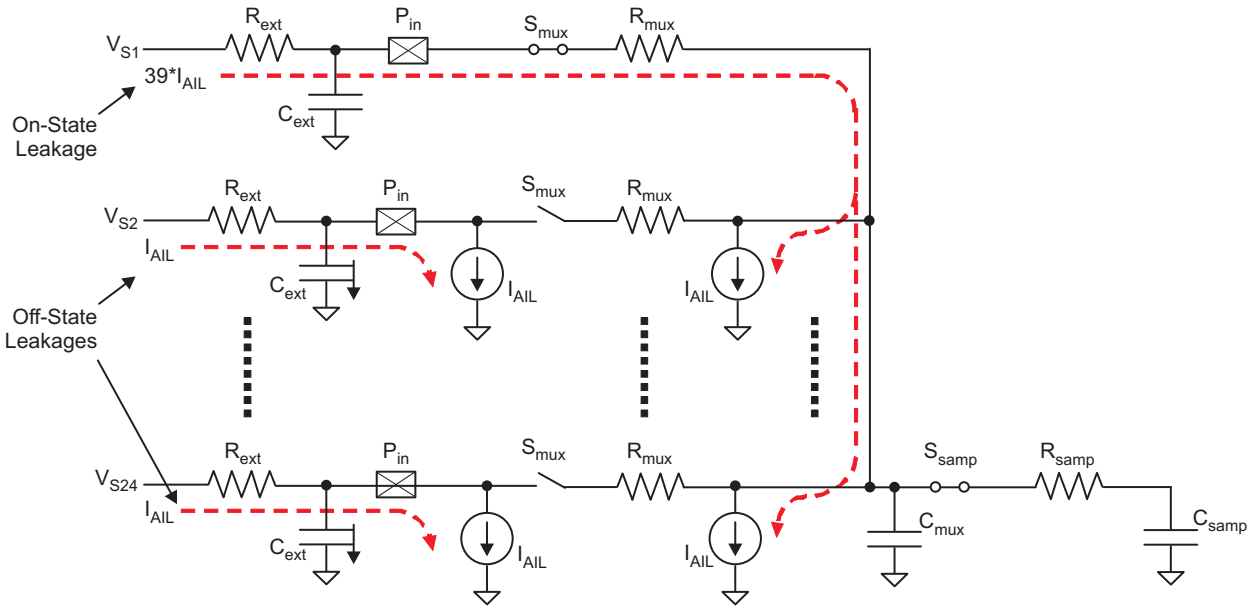

Figure 5-1. MibADC Input Equivalent Circuit

Table 5-7. MibADC Timing Specifications

Parameter		MIN	NOM	MAX	Unit
$t_{c(ADCLK)}$ (1)	Cycle time, MibADC clock	0.033			µs
$t_{d(SH)}$ (2)	Delay time, sample and hold time	0.2			µs
12-bit mode					
$t_{d©)}$	Delay time, conversion time	0.4			µs
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	0.6			µs
10-bit mode					
$t_{d©)}$	Delay time, conversion time	0.33			µs
$t_{d(SHC)}$ (4)	Delay time, total sample/hold and conversion time	0.53			µs

(1) The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.
(2) The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time needs to be determined by accounting for the external impedance connected to the input channel as well as the ADC's internal impedance.
(3) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, e.g the prescale settings.
(4) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, e.g the prescale settings.

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Table 5-8. MibADC Operating Characteristics Over Full Ranges of Recommended Operating Conditions

Parameter		Description/Conditions		MIN	Type	MAX	Unit
CR	Conversion range over which specified accuracy is maintained	AD_{REFHI} - AD_{REFLO}		3		5.5	V
Z_{SET}	Zero Scale Offset	Difference between the first ideal transition (from code 000h to 001h) and the actual transition	10-bit mode			1	LSB
			12-bit mode			2	LSB
F_{SET}	Full Scale Offset	Difference between the range of the measured code transitions (from first to last) and the range of the ideal code transitions	10-bit mode			2	LSB
			12-bit mode			3	LSB
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. (See Figure 76)	10-bit mode			± 1.5	LSB
			12-bit mode			± 2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error.	10-bit mode			± 2	LSB
			12-bit mode			± 2	LSB
E_{TOT}	Total unadjusted error (after calibration)	Maximum value of the difference between an analog value and the ideal midstep value.	10-bit mode			± 2	LSB
			12-bit mode			± 4	LSB

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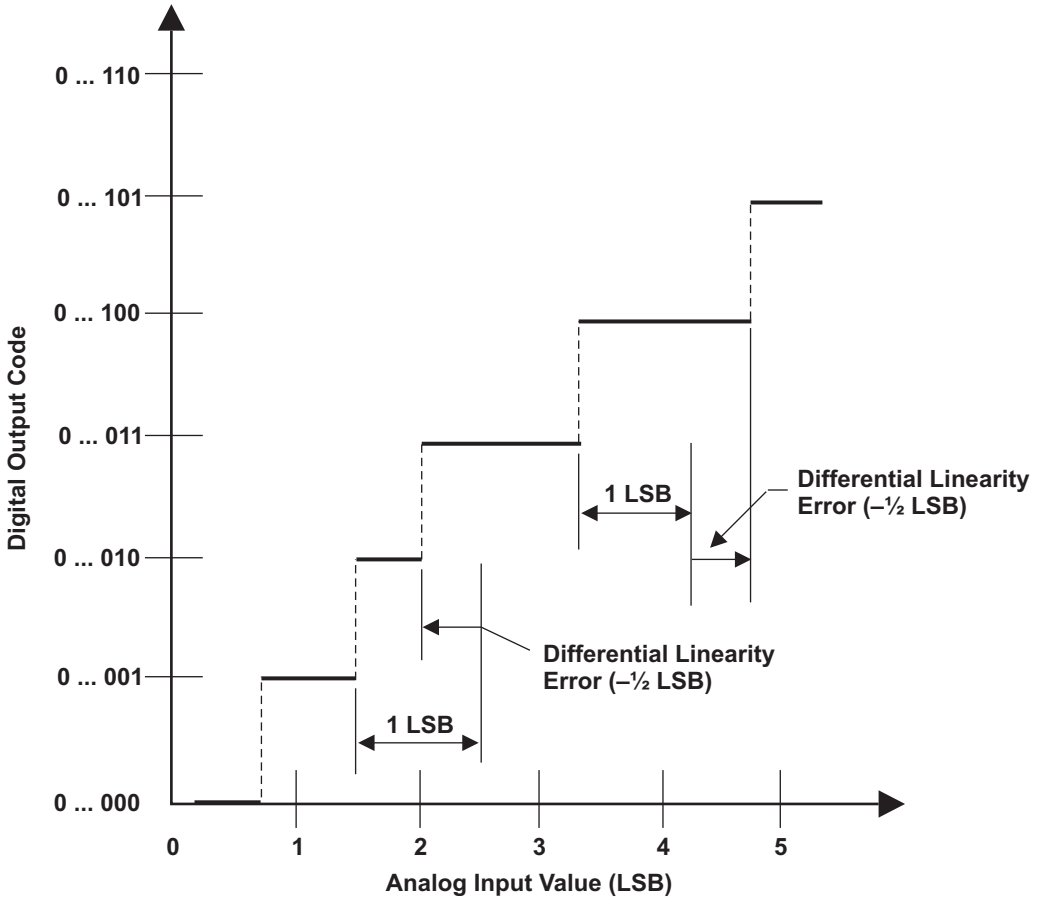
5.2.4 Performance (Accuracy) Specifications

5.2.4.1 MibADC Nonlinearity Errors

The differential nonlinearity error shown in Figure Figure 5-2 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

Figure 5-2. Differential Nonlinearity (DNL) Error

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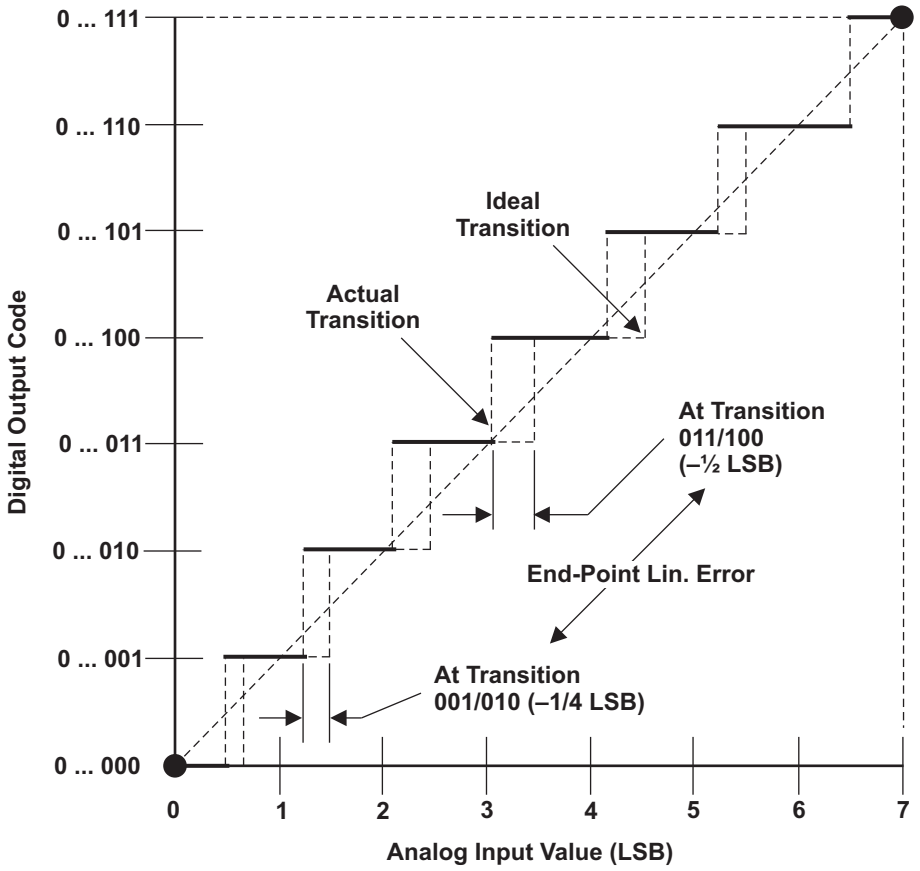
The integral nonlinearity error shown in Figure Figure 5-3 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

Figure 5-3. Integral Nonlinearity (INL) Error

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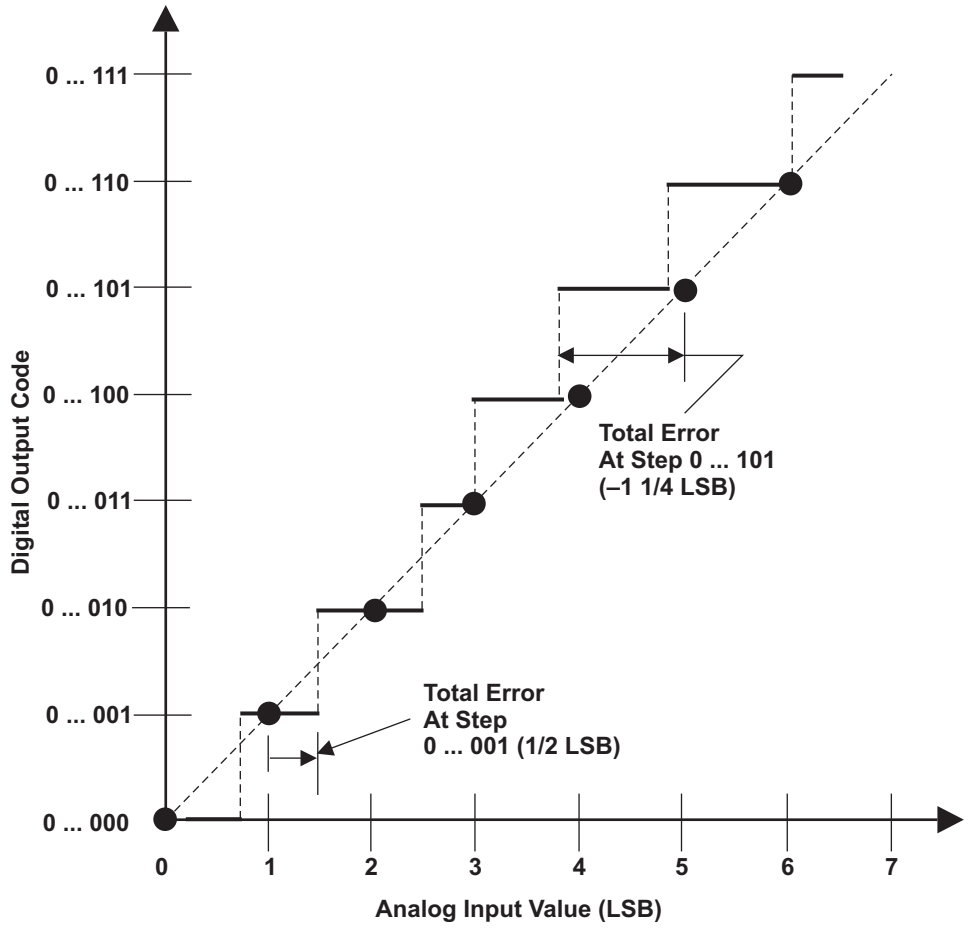
5.2.4.2 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in Figure Figure 5-4 is the maximum value of the difference between an analog value and the ideal midstep value.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

Figure 5-4. Absolute Accuracy (Total) Error

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5.3 General-Purpose Input/Output

The GPIO module on this device supports two ports, GIOA and GIOB. The I/O pins are bidirectional and bit-programmable. Both GIOA and GIOB support external interrupt capability.

5.3.1 Features

The GPIO module has the following features:

- Each IO pin can be configured as:
  - Input
  - Output
  - Open Drain
- The interrupts have the following characteristics:
  - Programmable interrupt detection either on both edges or on a single edge (set in GIOINTDET)
  - Programmable edge-detection polarity, either rising or falling edge (set in GIOPOL register)
  - Individual interrupt flags (set in GIOFLG register)
  - Individual interrupt enables, set and cleared through GIOENASET and GIOENACLR registers respectively
  - Programmable interrupt priority, set through GIOLVLSET and GIOLVLCLR registers
- Internal pullup/pulldown allows unused I/O pins to be left unconnected

For information on input and output timings see Section 3.8 and Section 3.9

5.4 Enhanced High-End Timer (N2HET)

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O.. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses.

5.4.1 Features

The N2HET module has the following features:

- Programmable timer for input and output timing functions
- Reduced instruction set (30 instructions) for dedicated time and angle functions
- 160 words of instruction RAM protected by parity
- User defined number of 25-bit virtual counters for timer, event counters and angle counters
- 7-bit hardware counters for each pin allow up to 32-bit resolution in conjunction with the 25-bit virtual counters
- Up to 32 pins usable for input signal measurements or output signal generation
- Programmable suppression filter for each input pin with adjustable limiting frequency
- Low CPU overhead and interrupt load
- Efficient data transfer to or from the CPU memory with dedicated High-End-Timer Transfer Unit (HTU) or DMA
- Diagnostic capabilities with different loopback mechanisms and pin status readback functionality

5.4.2 N2HET RAM Organization

The timer RAM uses 4 RAM banks, where each bank has two port access capability. This means that one RAM address may be written while another address is read. The RAM words are 96-bits wide, which are split into three 32-bit fields (program, control, and data).

5.4.3 Input Timing Specifications

The N2HET instructions PCNT and WCAP impose some timing constraints on the input signals.

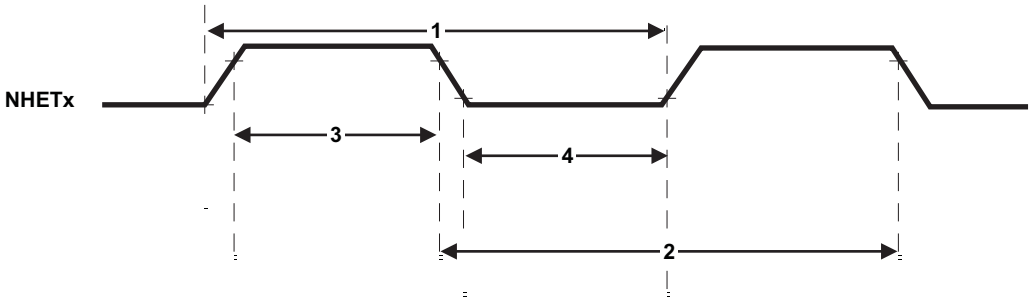

Figure 5-5. N2HET Input Capture Timings

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Table 5-9. Dynamic Characteristics for the N2HET Input Capture Functionality

	PARAMETER	MIN(1) (2)	MAX(1) (2)	UNIT
1	Input signal period, PCNT or WCAP for rising edge to rising edge	2 (hr) (lr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge	2 (hr) (lr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge	(hr) (lr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge	(hr) (lr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns

(1) hr = High-resolution prescaler, configured using the HRPFC field of the Prescale Factor Register (HETPFR).
(2) lr = Loop-resolution prescaler, configured using the LFPRC field of the Prescale Factor Register (HETPFR)

Both N2HET1 and N2HET2 have three channels each that are enhanced to be able to capture inputs with smaller pulse widths than that specified in Table 5-9. These are N2HET1 channels 15, 20 and 31, and N2HET2 channels 12, 14 and 16.

The input capture capability for these channels is specified in the following table.

Table 5-10. Input Capture Capability for N2HET Channels with Enhancements

	PARAMETER	MIN	MAX	UNIT
1	Input signal period, PCNT or WCAP for rising edge to rising edge	(hr) (lr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge	(hr) (lr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge	2 (hr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge	2 (hr) $tc_{(VCLK2)}$ + 2	2^{25} (hr) (lr) $tc_{(VCLK2)}$ - 2	ns

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5.4.4 N2HET1-N2HET2 Interconnections

In some applications the N2HET resolutions must be synchronized. Some other applications require a single time base to be used for all PWM outputs and input timing captures.

The N2HET provides such a synchronization mechanism. The Clk_master/slave (HETGCR.16) configures the N2HET in master or slave mode (default is slave mode). A N2HET in master mode provides a signal to synchronize the prescalers of the slave N2HET. The slave N2HET synchronizes its loop resolution to the loop resolution signal sent by the master. The slave does not require this signal after it receives the first synchronization signal. However, anytime the slave receives the re-synchronization signal from the master, the slave must synchronize itself again..

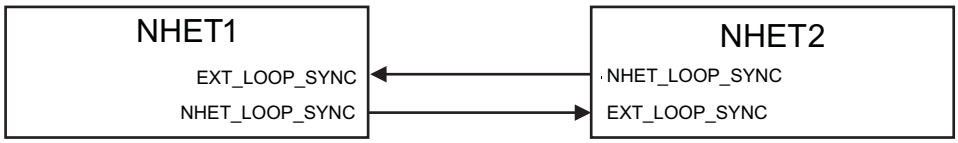

Figure 5-6. N2HET1 – N2HET2 Synchronization Hookup

5.4.5 N2HET Checking

5.4.5.1 Internal Monitoring

To assure correctness of the high-end timer operation and output signals, the two N2HET modules can be used to monitor each other's signals as shown in Figure 5-7. The direction of the monitoring is controlled by the I/O multiplexing control module.

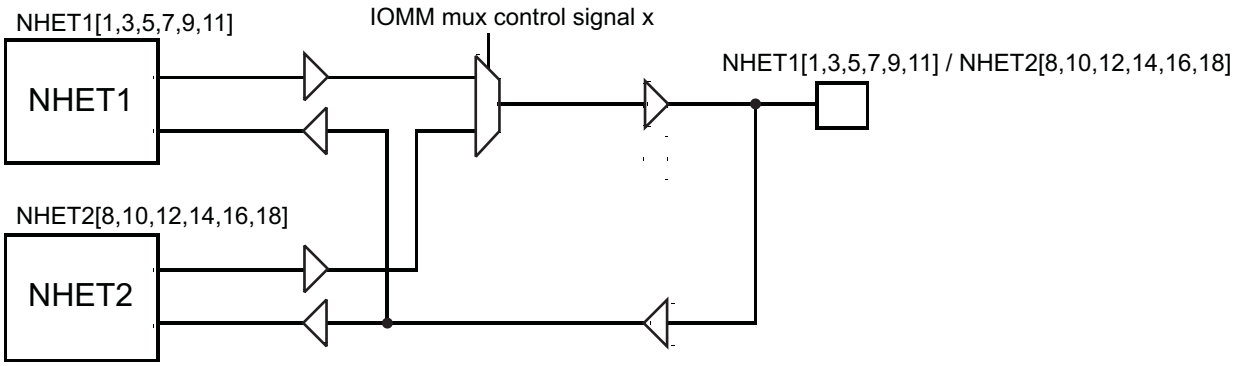

Figure 5-7. N2HET Monitoring

5.4.5.2 Output Monitoring using Dual Clock Comparator (DCC)

N2HET1[31] is connected as a clock source for counter 1 in DCC1. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET1[31].

Similarly, N2HET2[0] is connected as a clock source for counter 1 in DCC2. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET2[0].

Both N2HET1[31] and N2HET2[0] can be configured to be internal-only channels. That is, the connection to the DCC module is made directly from the output of the N2HETx module (from the input of the output buffer).

For more information on DCC see Section 4.7.3.

5.4.6 Disabling N2HET Outputs

Some applications require the N2HET outputs to be disabled under some fault condition. The N2HET module provides this capability via the "Pin Disable" input signal. This signal, when driven low, causes the N2HET outputs identified by a programmable register (HETPINDIS) to be tri-stated. Please refer to the for more details on the "N2HET Pin Disable" feature.

GIOA[5] is connected to the "Pin Disable" input for N2HET1, and GIOB[2] is connected to the "Pin Disable" input for N2HET2.

5.4.7 High-End Timer Transfer Unit (HET-TU)

A High End Timer Transfer Unit (HET-TU) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HET-TU.

5.4.7.1 Features

- CPU and DMA independent
- Master Port to access system memory
- 8 control packets supporting dual buffer configuration
- Control packet information is stored in RAM protected by parity
- Event synchronization (HET transfer requests)
- Supports 32 or 64 bit transactions
- Addressing modes for HET address (8 byte or 16 byte) and system memory address (fixed, 32 bit or 64bit)
- One shot, circular and auto switch buffer transfer modes
- Request lost detection

5.4.7.2 Trigger Connections

Table 5-11. HET TU1 Request Line Connection

Modules	Request Source	HET TU1 Request
N2HET1	HTUREQ[0]	HET TU1 DCP[0]
N2HET1	HTUREQ[1]	HET TU1 DCP[1]
N2HET1	HTUREQ[2]	HET TU1 DCP[2]
N2HET1	HTUREQ[3]	HET TU1 DCP[3]
N2HET1	HTUREQ[4]	HET TU1 DCP[4]
N2HET1	HTUREQ[5]	HET TU1 DCP[5]
N2HET1	HTUREQ[6]	HET TU1 DCP[6]
N2HET1	HTUREQ[7]	HET TU1 DCP[7]

Table 5-12. HET TU2 Request Line Connection

Modules	Request Source	HET TU2 Request
N2HET2	HTUREQ[0]	HET TU2 DCP[0]
N2HET2	HTUREQ[1]	HET TU2 DCP[1]
N2HET2	HTUREQ[2]	HET TU2 DCP[2]
N2HET2	HTUREQ[3]	HET TU2 DCP[3]
N2HET2	HTUREQ[4]	HET TU2 DCP[4]
N2HET2	HTUREQ[5]	HET TU2 DCP[5]
N2HET2	HTUREQ[6]	HET TU2 DCP[6]
N2HET2	HTUREQ[7]	HET TU2 DCP[7]

5.5 Controller Area Network (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

5.5.1 Features

Features of the DCAN module include:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- The CAN kernel can be clocked by the oscillator for baud-rate generation.
- 64 mailboxes on each DCAN
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM protected by parity
- Direct access to Message RAM during test mode
- CAN Rx / Tx pins configurable as general purpose IO pins
- Message RAM Auto Initialization
- DMA support

For more information on the DCAN see the RM48x Technical Reference Manual (SPNU481).

5.5.2 Electrical and Timing Specifications

Table 5-13. Dynamic Characteristics for the DCANx TX and RX pins

Parameter		MIN	MAX	Unit
$t_{d(CANnTX)}$	Delay time, transmit shift register to CANnTX pin(1)		15	ns
$t_{d(CANnRX)}$	Delay time, CANnRX pin to receive shift register		5	ns

(1) These values do not include rise/fall times of the output buffer.

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5.6 Local Interconnect Network Interface (LIN)

The SCI/LIN module can be programmed to work either as an SCI or as a LIN. The core of the module is an SCI. The SCI's hardware features are augmented to achieve LIN compatibility.

The SCI module is a universal asynchronous receiver-transmitter that implements the standard nonreturn to zero format. The SCI can be used to communicate, for example, through an RS-232 port or over a K-line.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multi-cast transmission between any network nodes.

5.6.1 LIN Features

The following are features of the LIN module:

- Compatible to LIN 1.3, 2.0 and 2.1 protocols
- Multi-buffered receive and transmit units DMA capability for minimal CPU intervention
- Identification masks for message filtering
- Automatic Master Header Generation
  - Programmable Synch Break Field
  - Synch Field
  - Identifier Field
- Slave Automatic Synchronization
  - Synch break detection
  - Optional baudrate update
  - Synchronization Validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Error detection
- 2 Interrupt lines with priority encoding

5.7 Serial Communication Interface (SCI)

5.7.1 Features

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard nonreturn to zero (NRZ) format
- Double-buffered receive and transmit functions
- Configurable frame format of 3 to 13 bits per character based on the following:
  - Data word length programmable from one to eight bits
  - Additional address bit in address-bit mode
  - Parity programmable for zero or one parity bit, odd or even parity
  - Stop programmable for one or two stop bits
- Asynchronous or isosynchronous communication modes
- Two multiprocessor communication formats allow communication between more than two devices.
- Sleep mode is available to free CPU resources during multiprocessor communication.
- The 24-bit programmable baud rate supports 2^{24} different baud rates provide high accuracy baud rate selection.
- Four error flags and Five status flags provide detailed information regarding SCI events.
- Capability to use DMA for transmit and receive data.

5.8 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module is a multi-master communication module providing an interface between the RM4x microcontroller and devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I2C-bus. This module will support any slave or master I2C compatible device.

5.8.1 Features

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 10 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Seven interrupts that can be used by the CPU
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

NOTE

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

5.8.2 I2C I/O Timing Specifications

Table 5-14. I2C Signals (SDA and SCL) Switching Characteristics(1)

Parameter		Standard Mode		Fast Mode		Unit
		MIN	MAX	MIN	MAX	
$t_{c(I2CCLK)}$	Cycle time, Internal Module clock for I2C, prescaled from VCLK	75.2	149	75.2	149	ns
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		ms
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		ms
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a repeated START condition)	4		0.6		ms
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		ms
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		ms
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low (for I2C bus devices)	0	3.45(2)	0	0.9	ms
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		ms
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4.0		0.6		ms
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b(3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) C_b = The total capacitance of one bus line in pF.

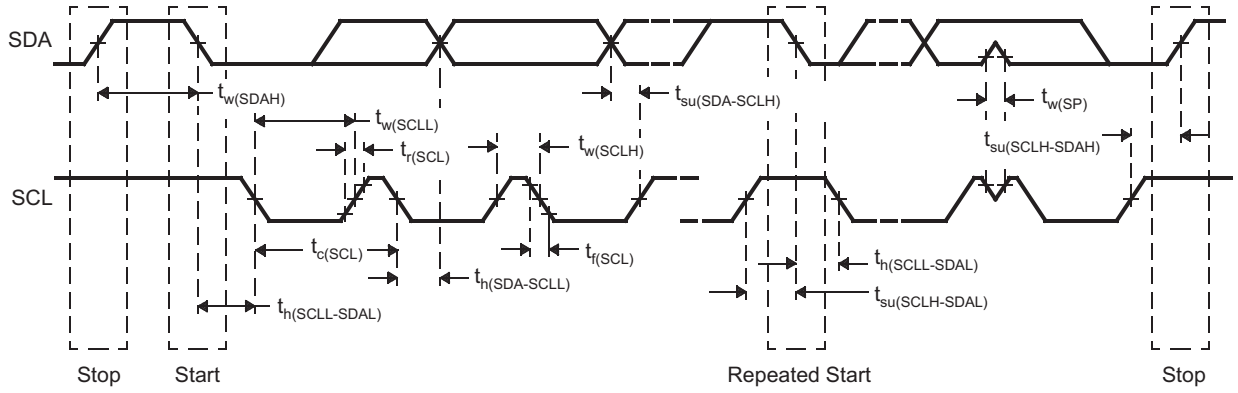

Figure 5-8. I2C Timings

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NOTE

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.
- A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.
- C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

5.9 Multi-Buffered / Standard Serial Peripheral Interface

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications for the SPI include interfacing to external peripherals, such as I/Os, memories, display drivers, and analog-to-digital converters.

5.9.1 Features

Both Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator, supports max up to 20Mhz baud rate
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format
- SPI I/Os not used in the communication can be used as digital input/output signals

Table 5-15. MibSPI/SPI Configurations

MibSPIx/SPIx	I/Os
MibSPI1	MIBSPI1SIMO[1:0], MIBSPI1SOMI[1:0], MIBSPI1CLK, MIBSPI1nCS[5:0], MIBSPI1nENA
MibSPI3	MIBSPI3SIMO, MIBSPI3SOMI, MIBSPI3CLK, MIBSPI3nCS[5:0], MIBSPI3nENA
MibSPI5	MIBSPI5SIMO[3:0], MIBSPI5SOMI[3:0], MIBSPI5CLK, MIBSPI5nCS[3:0], MIBSPI5nENA
SPI2	SPI2SIMO, ZSPI2SOMI, SPI2CLK, SPI2nCS[1:0], SPI2nENA
SPI4	SPI4SIMO, SPI4SOMI, SPI4CLK, SPI4nCS[0], SPI4nENA

5.9.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 128 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

5.9.3 MibSPI Transmit Trigger Events

Each of the transfer groups can be configured individually. For each of the transfer groups a trigger event and a trigger source can be chosen. A trigger event can be for example a rising edge or a permanent low level at a selectable trigger source. For example, up to 15 trigger sources are available which can be utilized by each transfer group. These trigger options are listed in Table 5-16 and Section 5.9.3.2 for MibSPI1 and MibSPi3 respectively.

5.9.3.1 MIBSPI1 Event Trigger Hookup

Table 5-16. MIBSPI1 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET1[8]
EVENT9	1010	N2HET1[10]
EVENT10	1011	N2HET1[12]
EVENT11	1100	N2HET1[14]
EVENT12	1101	N2HET1[16]
EVENT13	1110	N2HET1[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET1 trigger sources, the connection to the MibSPI1 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

NOTE

For GIOx trigger sources, the connection to the MibSPI1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin, or by driving the GIOx pin from an external trigger source.

5.9.3.2 MIBSPI3 Event Trigger Hookup

Table 5-17. MIBSPI3 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	HET[8]
EVENT9	1010	N2HET1[10]
EVENT10	1011	N2HET1[12]
EVENT11	1100	N2HET1[14]

Table 5-17. MIBSPI3 Event Trigger Hookup (continued)

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
EVENT12	1101	N2HET1[16]
EVENT13	1110	N2HET1[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET1 trigger sources, the connection to the MibSPI3 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

NOTE

For GIOx trigger sources, the connection to the MibSPI3 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin, or by driving the GIOx pin from an external trigger source.

5.9.3.3 MIBSPI5 Event Trigger Hookup

Table 5-18. MIBSPI5 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET1[8]
EVENT9	1010	N2HET1[10]
EVENT10	1011	N2HET1[12]
EVENT11	1100	N2HET1[14]
EVENT12	1101	N2HET1[16]
EVENT13	1110	N2HET1[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET1 trigger sources, the connection to the MibSPI5 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

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NOTE

For GIOx trigger sources, the connection to the MibSPI5 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin + selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI5 transfers; there is no multiplexing on the input connections.

5.9.4 MibSPI/SPI Master Mode I/O Timing Specifications

Table 5-19. SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	Parameter			MIN	MAX	Unit
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		40	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 5$		ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 5$		
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 3$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 3$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		$0.5t_{f(SPC)} + 2$		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		$0.5t_{f(SPC)} + 2$		
7(5)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		5		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		5		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 15$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 15$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 15$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 3$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 15$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 3$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low CS until inactive (clock polarity = 0)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 5$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 8$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + tr(SPICS) - 5$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 8$	ns
10	t_{SPIENA}	SPIENAn Sample point		$(C2TDELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} - 25$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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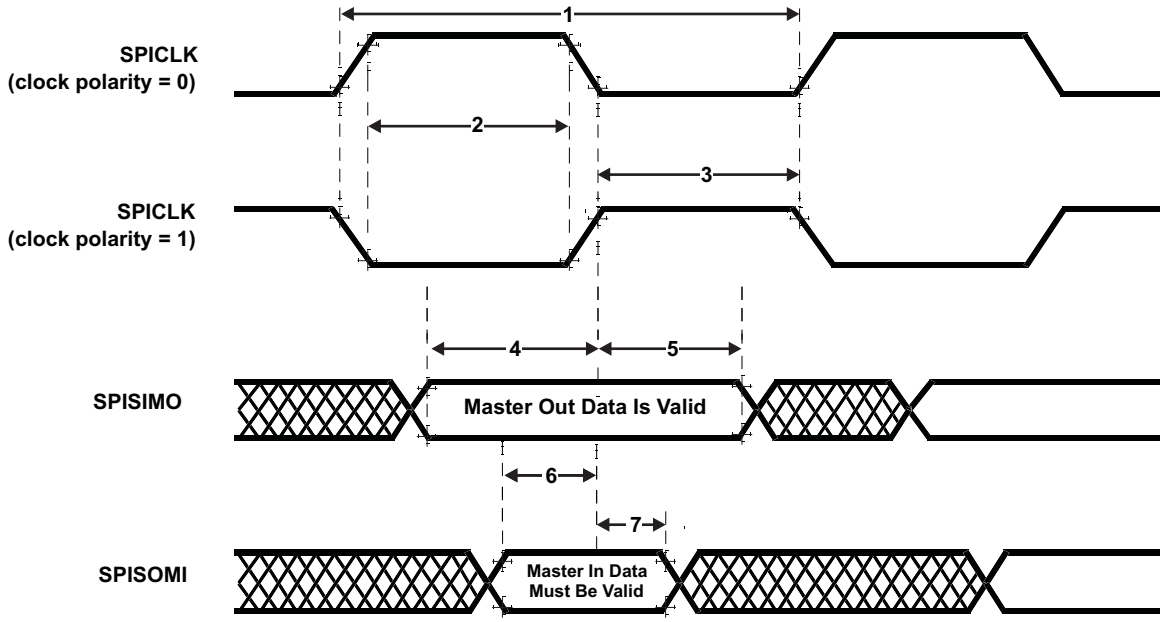

Figure 5-9. SPI Master Mode External Timing (CLOCK PHASE = 0)

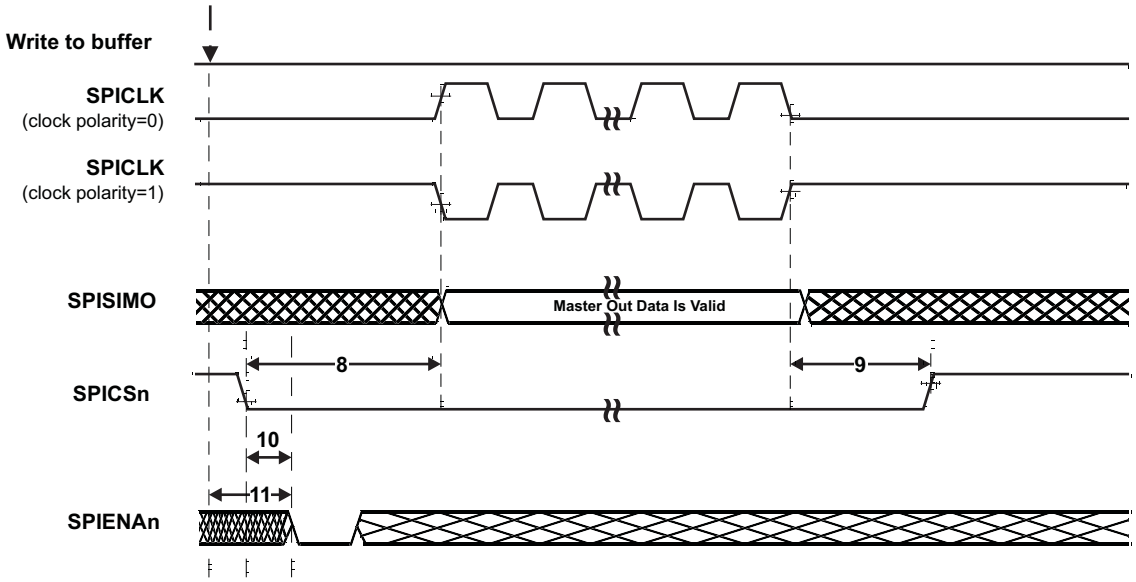

Figure 5-10. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

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Table 5-20. SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	Parameter			MIN	MAX	Unit
1	$t_{c(SPC)M}$	Cycle time, SPICLK (4)		40	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0)		$0.5t_{c(SPC)M} - 5$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1)		$0.5t_{c(SPC)M} - 5$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 3$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 3$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)		$t_{r(SPC)}$		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)		$t_{f(SPC)}$		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)		5		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)		5		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 15$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 15$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 15$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 3$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 15$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 3$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low CS until inactive (clock polarity = 0)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 4$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 8$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 4$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 8$	ns
10	t_{SPIENA}	SPIENAn Sample Point		$(C2TDELAY+1)* t_{c(VCLK)} - t_{f(SPICS)} - 25$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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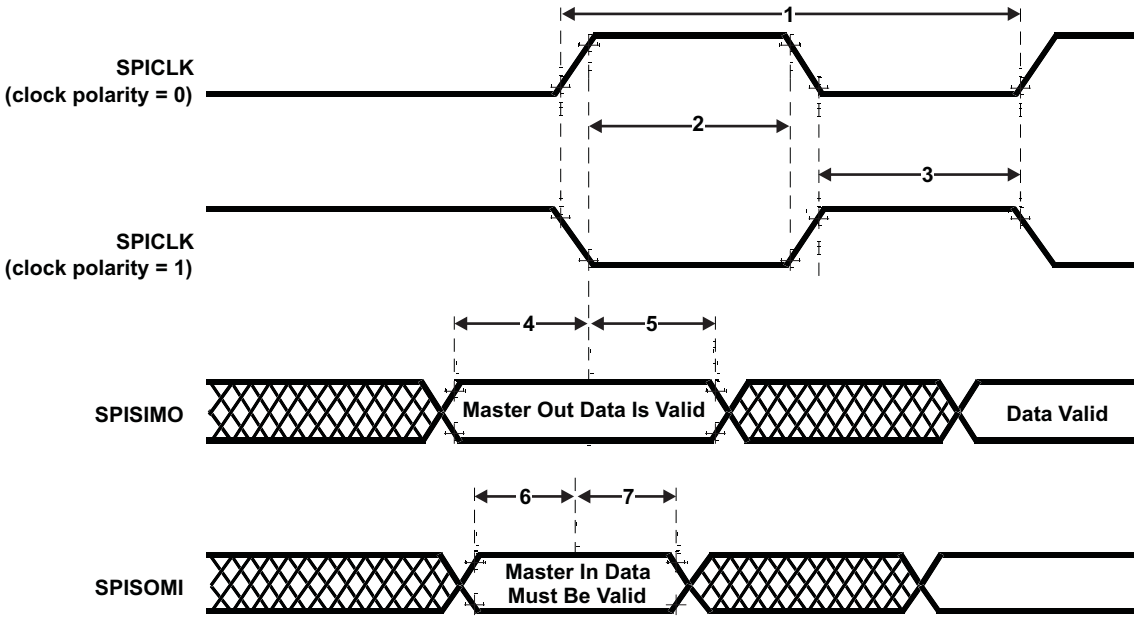

Figure 5-11. SPI Master Mode External Timing (CLOCK PHASE = 1)

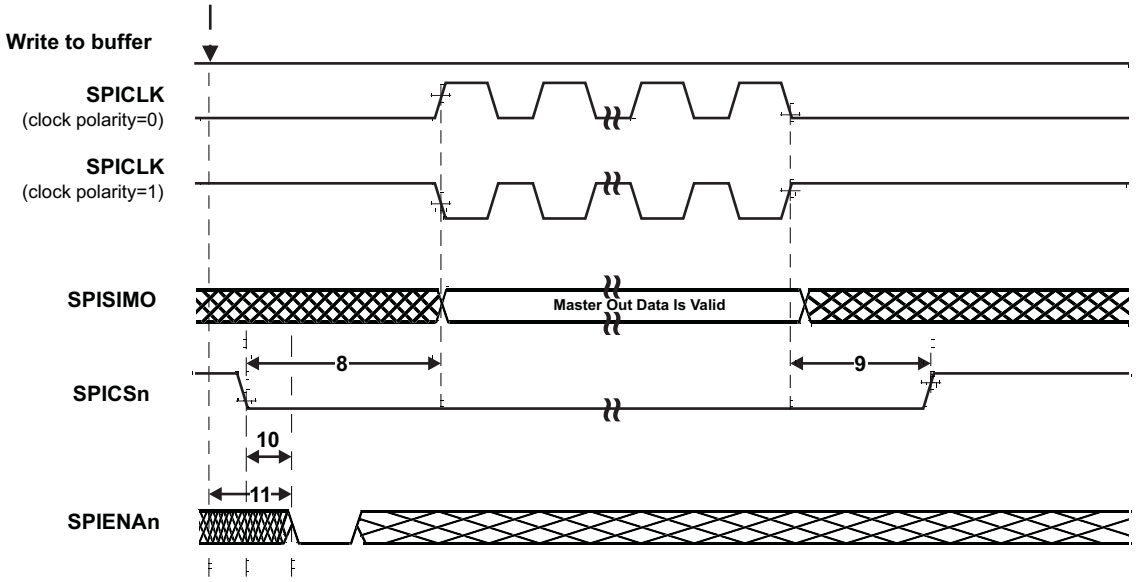

Figure 5-12. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

5.9.5 SPI Slave Mode I/O Timings

Table 5-21. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	40	$256t_{c(VCLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)		$t_{rf(SOMI)}$ + 18	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)		$t_{rf(SOMI)}$ + 18	
5(6)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	2		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	2		
7(6)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	2		ns
	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after S PICLK high (clock polarity = 1)	2		
8	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	ns
	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}+14$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
(4) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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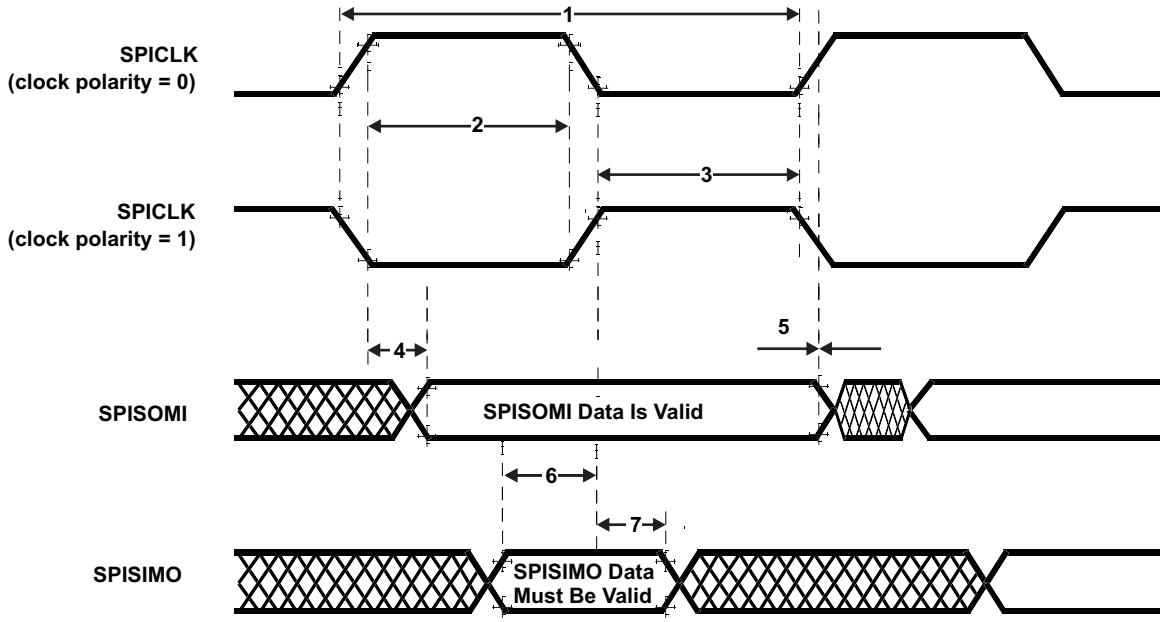

Figure 5-13. SPI Slave Mode External Timing (CLOCK PHASE = 0)

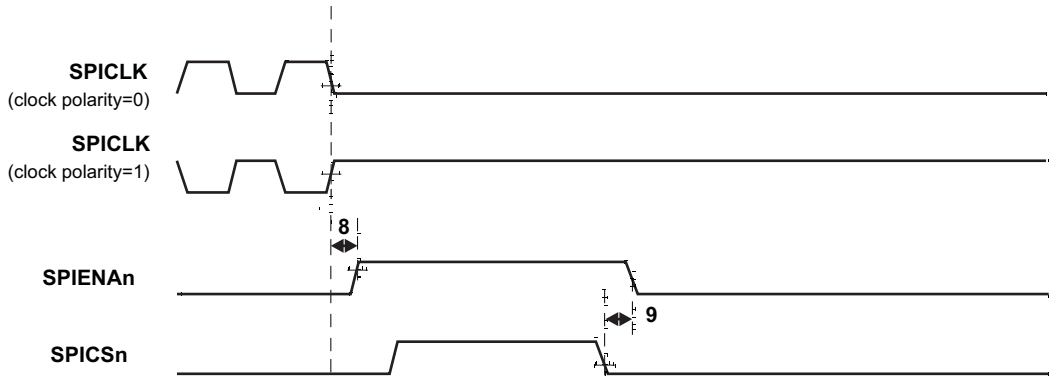

Figure 5-14. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

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Table 5-22. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	40	$256t_{c(VCLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SOMI-SPCL)S}$	Dealy time, SPISOMI data valid after SPICLK low (clock polarity = 0)		$t_{rf(SOMI)}$ + 18	ns
	$t_{d(SOMI-SPCH)S}$	Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1)		$t_{rf(SOMI)}$ + 18	
5(6)	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	2		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	2		
7(6)	$t_{v(SPCH-SIMO)S}$	High time, SPISIMO data valid after SPICLK high (clock polarity = 0)	2		ns
	$t_{v(SPCL-SIMO)S}$	High time, SPISIMO data valid after SPICLK low (clock polarity = 1)	2		
8	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	ns
	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}+14$	ns
10	$t_{d(SCSL-SOMI)S}$	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)	$t_{c(VCLK)}$	$2t_{c(VCLK)}+t_{rf(SOMI)}+8$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: tc(SPC)S ≤ (PS + 1) tc(VCLK), where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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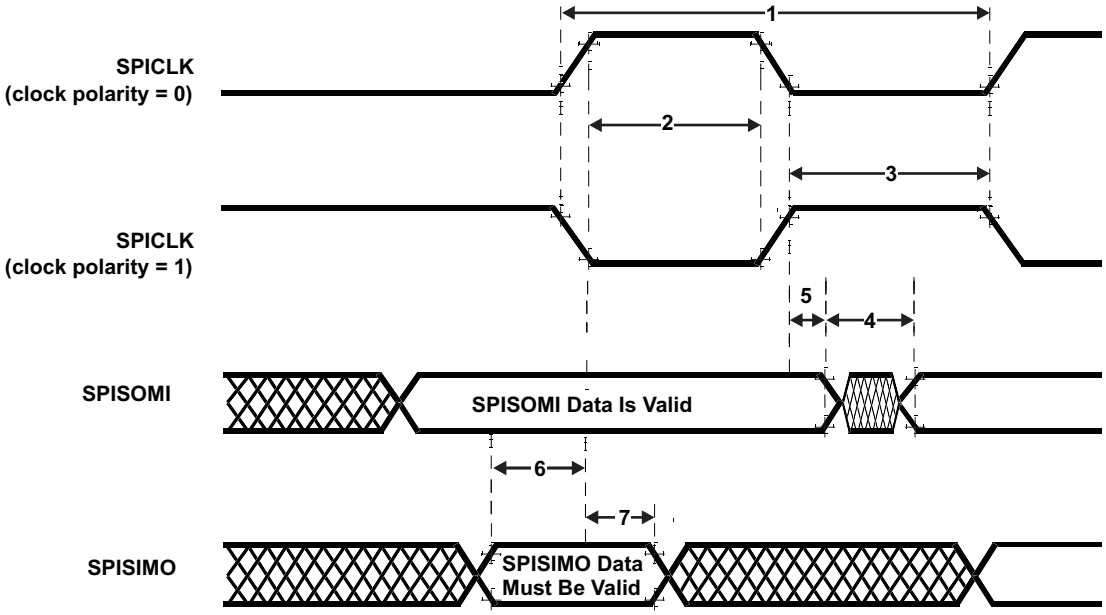

Figure 5-15. SPI Slave Mode External Timing (CLOCK PHASE = 1)

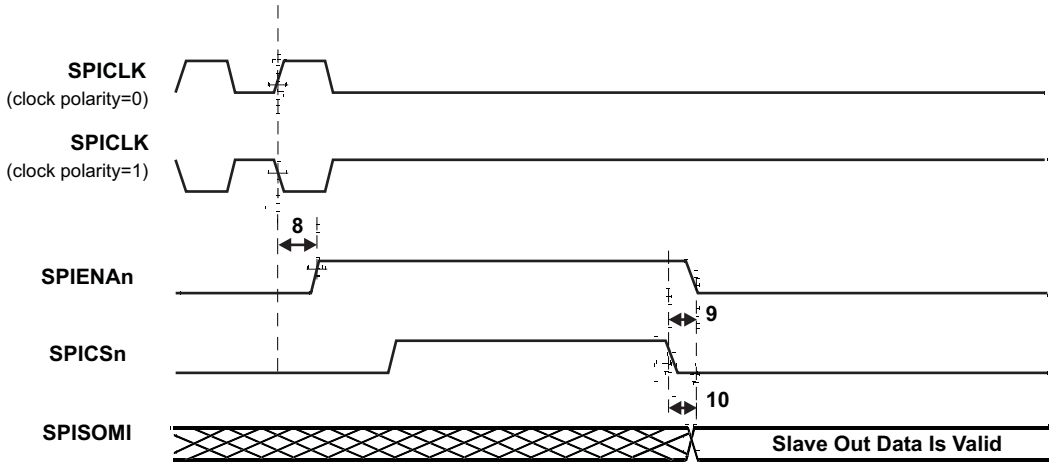

Figure 5-16. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

5.10 Ethernet Media Access Controller

The Ethernet Media Access Controller (EMAC) provides an efficient interface between and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QoS) support.

The EMAC controls the flow of packet data from the device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

5.10.1 Ethernet MII Electrical and Timing Specifications

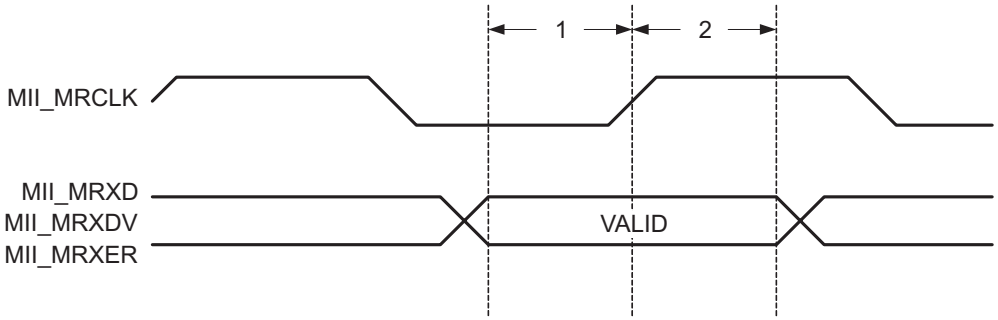

Figure 5-17. MII Receive Timing

Table 5-23. MII Receive Timing

Parameter	Description	MIN	MAX
$t_{su(GMIIMRXD)}$	Setup time, GMIIMRXD to GMIIMRCLK rising edge	8ns	
$t_{su(GMIIMRXDV)}$	Setup time, GMIIMRXDV to GMIIMRCLK rising edge	8ns	
$t_{su(GMIIMRXER)}$	Setup time, GMIIMRXER to GMIIMRCLK rising edge	8ns	
$t_{h(GMIIMRXD)}$	Hold time, GMIIMRXD valid after GMIIRCLK rising edge	8ns	
$t_{h(GMIIMRXDV)}$	Hold time, GMIIMRXDV valid after GMIIRCLK rising edge	8ns	
$t_{h(GMIIMRXER)}$	Hold time, GMIIMRXDV valid after GMIIRCLK rising edge	8ns	

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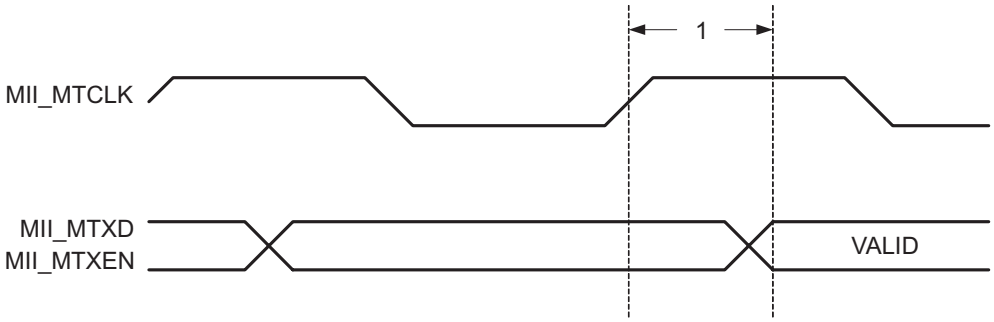

Figure 5-18. MII Transmit Timing

Table 5-24. MII Transmit Timing

Parameter	Description	MIN	MAX
$t_{d(GMIIMTXD)}$	Delay time, GMIIMTCLK rising edge to GMIIMTXD	5ns	25ns
$t_{d(GMIIMTXEN)}$	Delay time, GMIIMTCLK rising edge to GMIIMTXEN	5ns	25ns

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5.10.2 Management Data Input/Output (MDIO)

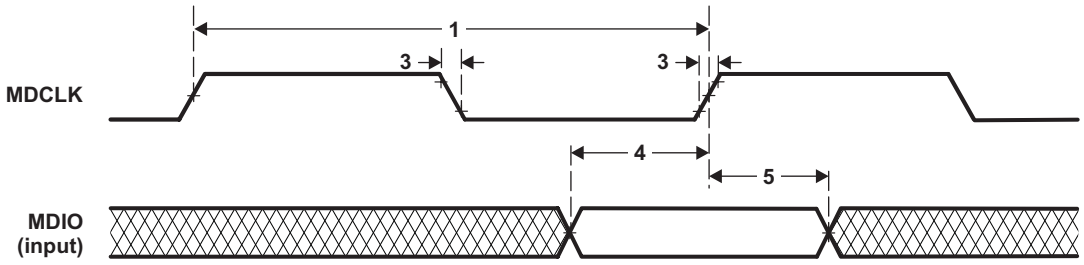

Figure 5-19. MDIO Input Timing

Table 5-25. MDIO Input Timing Requirements

NO.	Parameter		Value		Unit
			MIN	MAX	
1	tc(MDCLK)	Cycle time, MDCLK	400	-	ns
2	tw(MDCLK)	Pulse duration, MDCLK high/low	180	-	ns
3	tt(MDCLK)	Transition time, MDCLK	-	5	ns
4	tsu(MDIO-MDCLKH)	Setup time, MDIO data input valid before MDCLK High	10	-	ns
5	th(MDCLKH-MDIO)	Hold time, MDIO data input valid after MDCLK High	10	-	ns

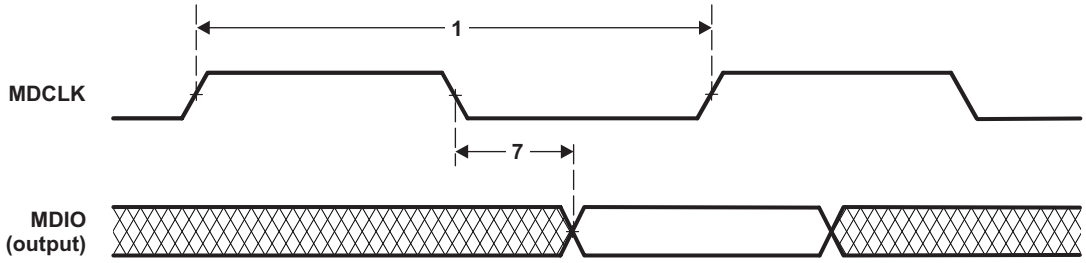

Figure 5-20. MDIO Output Timing

Table 5-26. MDIO Output Timing Requirements

NO.	Parameter		Value		Unit
			MIN	MAX	
1	tc(MDCLK)	Cycle time, MDCLK	400	-	ns
7	td(MDCLKL-MDIO)	Delay time, MDCLK low to MDIO data output valid	0	100	ns

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6 Mechanical Data

6.1 Thermal Data

Table 6-1 shows the thermal resistance characteristics for the QFP - PGE mechanical package.

Table 6-2 shows the thermal resistance characteristics for the BGA - ZWT mechanical package.

Table 6-1. Thermal Resistance Characteristics (PGE Package)

PARAMETER	°C / W
$R\Theta_{JA}$	45
$R\Theta_{JC}$	5

Table 6-2. Thermal Resistance Characteristics (ZWT Package)

PARAMETER	°C / W
$R\Theta_{JA}$	18.8
$R\Theta_{JC}$	7.1

6.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

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