TEXAS INSTRUMENTS

TUSB2136

Universal Serial Bus Keyboard Hub Controller

Data Manual

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SLLS442B

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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1 Introduction

The TUSB2136 is an integrated universal serial bus (USB) 1.1 hub with a keyboard I/O controller. This makes it an ideal solution for a compound USB keyboard with built-in hub device. The TUSB2136 has 8k × 8 RAM space for application development. A ROM based version of the TUSB2136 has 8k × 8 ROM space for predeveloped customer specific production applications. In addition, the TUSB2136 is programmable and may be used for various other general USB controller applications. Unique vendor identification and product identification (VID/PID) may be selected without the use of an external EEPROM. Using a 12 MHz crystal, the onboard oscillator generates the internal system clocks. No additional programming is required for any part of the hub functions. The device may be programmed via an inter-IC (I^2C) serial interface at power on from an EEPROM, or optionally, the application firmware may be downloaded from a host PC via USB. The 8052-based microprocessor allows several third party standard tools to be used for application development. In addition, the application code available in the general market may also be utilized (this may or may not require some code modification due to hardware variations).

1.1 Features

- Multiproduct support with one code and one chip (up to 16 products with one chip)
- Fully compliant with the USB release 1.1 specification
- Supports 1.5 and 12 Mbits/s USB data rate
- Supports USB suspend/resume and remote wake-up operation
- Integrated two-port hub with individual power management per port
- Integrated 8052 microcontroller with:
  - 256 × 8 RAM for internal data
  - 8k × 8 RAM code space available for downloadable firmware from host or I^2C port. [1]
  - 512 × 8 shared RAM used for data buffers and endpoint descriptor blocks (EDB) [2]
  - Four 8052 GPIO ports, Port 0,1, 2 and 3
  - Master I^2C controller for external slave device access
  - Watchdog timer
- Operates from a 12 MHz crystal
- On-chip PLL generates 48/12 MHz
- Supports a total of 4 input and 4 output endpoints
- Power-down mode
- 3.3-V operation
- 64-pin TQFP package

[1] The TUSB2136 has 8K x 8 RAM for development. 8K x 8 ROM version available. Contact TI Marketing

[2] This is the buffer space for USB packet transactions.

1.2 Functional Block Diagram

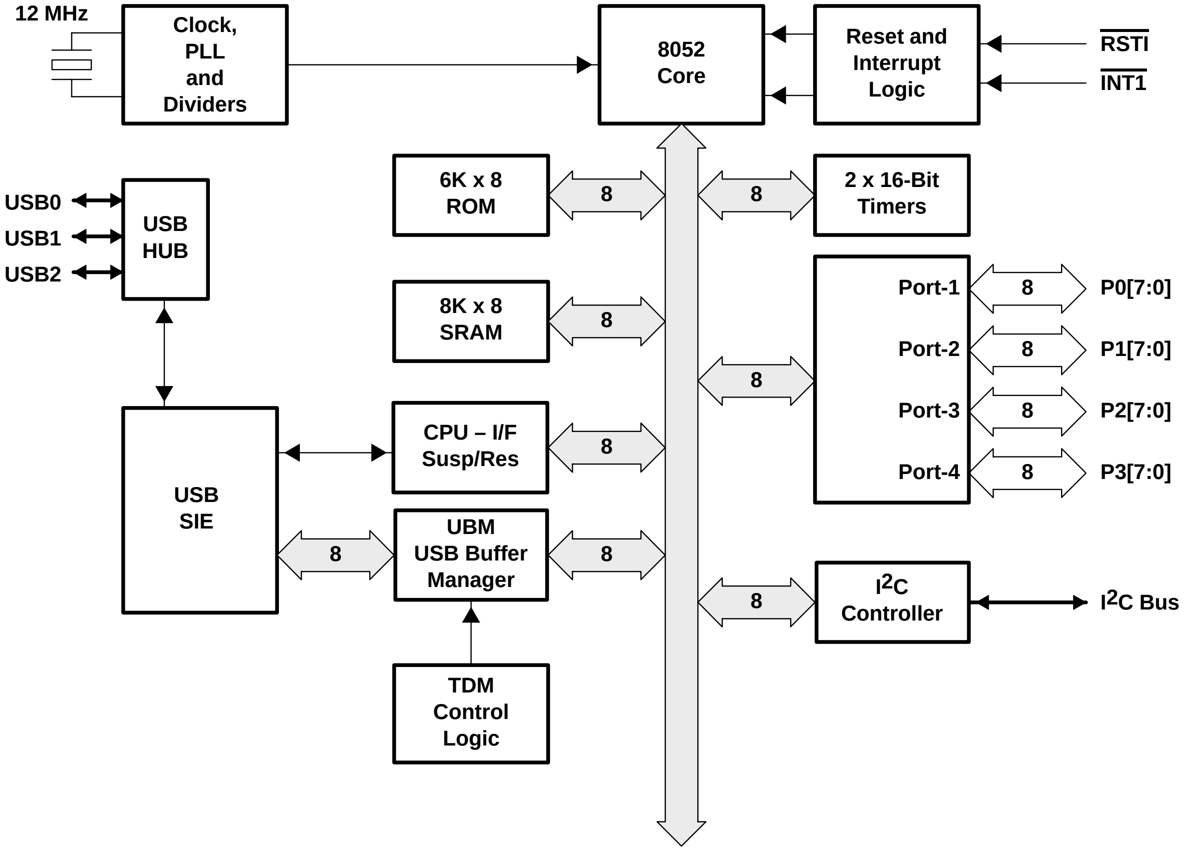
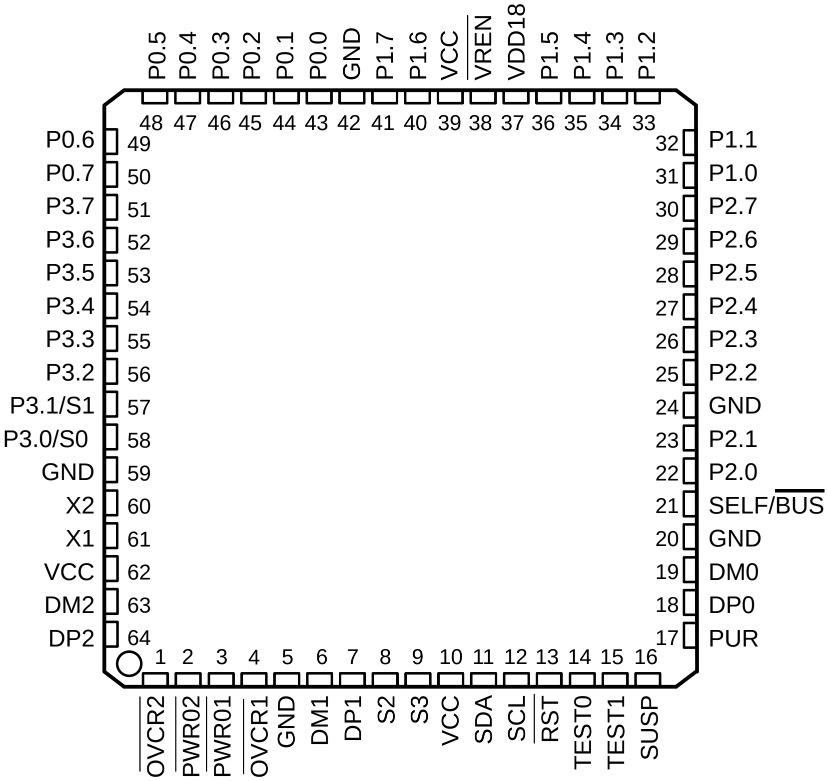


Figure 1–1. TUSB2136 Block Diagram

1.3 Terminal Assignments

PM PACKAGE
(TOP VIEW)



1.4 Ordering Information

T_A	PACKAGE
	PLASTIC QUAD FLATPACK (PM)
0°C to 70°C	TUSB2136PM

1.5 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DM0	19	I/O	Differential data minus USB port 0: upstream
DM1	6	I/O	Differential data minus Port-1: downstream
DM2	63	I/O	Differential data minus Port-2: downstream
DP0	18	I/O	Differential data plus USB port 0: upstream
DP1	7	I/O	Differential data plus Port-1: downstream
DP2	64	I/O	Differential data plus Port-2: downstream
GND	5,20,24,42,59	I	Power supply ground
$\overline{\text{OVCR1}}$	4	I	Port-1: Overcorrect indicator; Schmitt-trigger input, 100 μA active pullup
$\overline{\text{OVCR2}}$	1	I	Port-2: Overcorrect indicator; Schmitt-trigger input, 100 μA active pullup
P0.0	43	I/O	General-purpose I/O port 0 bit 0, Schmitt-trigger input 100 μA active pullup, open drain output
P0.1	44	I/O	General-purpose I/O port 0 bit 1, Schmitt-trigger input 100 μA active pullup, open drain output
P0.2	45	I/O	General-purpose I/O port 0 bit 2, Schmitt-trigger input 100 μA active pullup, open drain output
P0.3	46	I/O	General-purpose I/O port 0 bit 3, Schmitt-trigger input 100 μA active pullup, open drain output
P0.4	47	I/O	General-purpose I/O port 0 bit 4, Schmitt-trigger input 100 μA active pullup, open drain output
P0.5	48	I/O	General-purpose I/O port 0 bit 5, Schmitt-trigger input 100 μA active pullup, open drain output
P0.6	49	I/O	General-purpose I/O port 0 bit 6, Schmitt-trigger input 100 μA active pullup, open drain output
P0.7	50	I/O	General-purpose I/O port 0 bit 7, Schmitt-trigger input 100 μA active pullup, open drain output
P1.0	31	I/O	General-purpose I/O port 1 bit 0, Schmitt-trigger input 100 μA active pullup, open drain output
P1.1	32	I/O	General-purpose I/O port 1 bit 1, Schmitt-trigger input 100 μA active pullup, open drain output
P1.2	33	I/O	General-purpose I/O port 1 bit 2, Schmitt-trigger input 100 μA active pullup, open drain output
P1.3	34	I/O	General-purpose I/O port 1 bit 3, Schmitt-trigger input 100 μA active pullup, open drain output
P1.4	35	I/O	General-purpose I/O port 1 bit 4, Schmitt-trigger input 100 μA active pullup, open drain output
P1.5	36	I/O	General-purpose I/O port 1 bit 5, Schmitt-trigger input 100 μA active pullup, open drain output
P1.6	40	I/O	General-purpose I/O port 1 bit 6, Schmitt-trigger input 100 μA active pullup, open drain output
P1.7	41	I/O	General-purpose I/O port 1 bit 7, Schmitt-trigger input 100 μA active pullup, open drain output
P2.0	22	I/O	General-purpose I/O port 2 bit 0, Schmitt-trigger input 100 μA active pullup, open drain output
P2.1	23	I/O	General-purpose I/O port 2 bit 1, Schmitt-trigger input 100 μA active pullup, open drain output
P2.2	25	I/O	General-purpose I/O port 2 bit 2, Schmitt-trigger input 100 μA active pullup, open drain output
P2.3	26	I/O	General-purpose I/O port 2 bit 3, Schmitt-trigger input 100 μA active pullup, open drain output
P2.4	27	I/O	General-purpose I/O port 2 bit 4, Schmitt-trigger input 100 μA active pullup, open drain output
P2.5	28	I/O	General-purpose I/O port 2 bit 5, Schmitt-trigger input 100 μA active pullup, open drain output
P2.6	29	I/O	General-purpose I/O port 2 bit 6, Schmitt-trigger input 100 μA active pullup, open drain output
P2.7	30	I/O	General-purpose I/O port 2 bit 7, Schmitt-trigger input 100 μA active pullup, open drain output
P3.0/S0	58	I/O	General-purpose I/O port 3 bit 0, Schmitt-trigger input 100 μA active pullup, open drain output
P3.1/S1	57	I/O	General-purpose I/O port 3 bit 1, Schmitt-trigger input 100 μA active pullup, open drain output
P3.2	56	I/O	General-purpose I/O port 3 bit 2,
P3.3	55	I/O	General-purpose I/O port 3 bit 3, Schmitt-trigger input 100 μA active pullup, open drain output will not support $\overline{\text{INT1}}$ input
P3.4	54	I/O	General-purpose I/O port 3 bit 4, Schmitt-trigger input 100 μA active pullup, open drain output
P3.5	53	I/O	General-purpose I/O port 3 bit 5, Schmitt-trigger input 100 μA active pullup, open drain output
P3.6	52	I/O	General-purpose I/O port 3 bit 6, Schmitt-trigger input 100 μA active pullup, open drain output
P3.7	51	I/O	General-purpose I/O port 3 bit 7, Schmitt-trigger input 100 μA active pullup, open drain output
PUR	17	O	Pullup resistor connection pin (3-state) push-pull CMOS output (±8 mA)
$\overline{\text{PWRO1}}$	3	O	Port-1: power on/off control signal; push-pull CMOS output (±8mA)

1.5 Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{PWRO2}}$	2	O	Port-2: power on/off control signal; push-pull CMOS output (±8mA)
$\overline{\text{RST}}$	13	I	Controller master reset signal, Schmitt-trigger input 100 µA active pullup
S2	8	I	VID/PID selection pin
S3	9	I	VID/PID selection pin
SCL	12	O	Serial clock I^2C; open drain output
SDA	11	I/O	Serial data I^2C; open drain output
SELF/$\overline{\text{BUS}}$	21	I	USB power MODE select: self-powered (HIGH), bus-powered (LOW)
SUSP	16	O	Suspend status signal: suspended (HIGH); unsuspended (LOW)
TEST0	14	I	Test input0, Schmitt-trigger input 100 µA active pullup
TEST1	15	I	Test input1, Schmitt-trigger input 100 µA active pullup
VCC	10,39,62	I	Power supply input 3.3 V typical
VDD18	37		1.8-V power supply. An internal voltage regulator generates this supply voltage when terminal $\overline{\text{VREN}}$ is asserted. When $\overline{\text{VREGEN}}$ is deasserted, 1.8 V must be supplied externally.
$\overline{\text{VREN}}$	38	I	Voltage regulator enable: enable active LOW; disable active HIGH
X2	60	O	12-MHz crystal output
X1	61	I	12-MHz crystal input

NOTE 1: The MCU treats the outputs as open drain types in that the output can be driven low continuously, but a high output is driven for two clock cycles and then the output is tristated.

2 Functional Description

2.1 MCU Memory Map

Figure 2–1 illustrates the MCU memory map under boot and normal operation. It must be noted that the internal 256 bytes of IDATA are not shown since it is assumed to be in the standard 8052 location (0000 to 00FF). The shaded areas represent the internal ROM/RAM. For more information regarding the integrated 8052, see the *TUSBxxxx Microcontroller Reference Guide* (SLLU044).

When SDW bit = 0 (Boot mode): The 6k-ROM is mapped to address (0000–17FF) and is duplicated in location (8000–97FF) in code space. The internal 8k-RAM is mapped to address range (0000–1FFF) in data space. Buffers, MMR and I/O are mapped to address range (FD80–FFFF) in data space.

When SDW bit = 1 (Normal mode): The 6k-ROM is mapped to (8000–97FF) in code space. The internal 8k-RAM is mapped to address range (0000–1FFF) code space. Buffers, MMR and I/O are mapped to address range (FD80–FFFF) in data space.

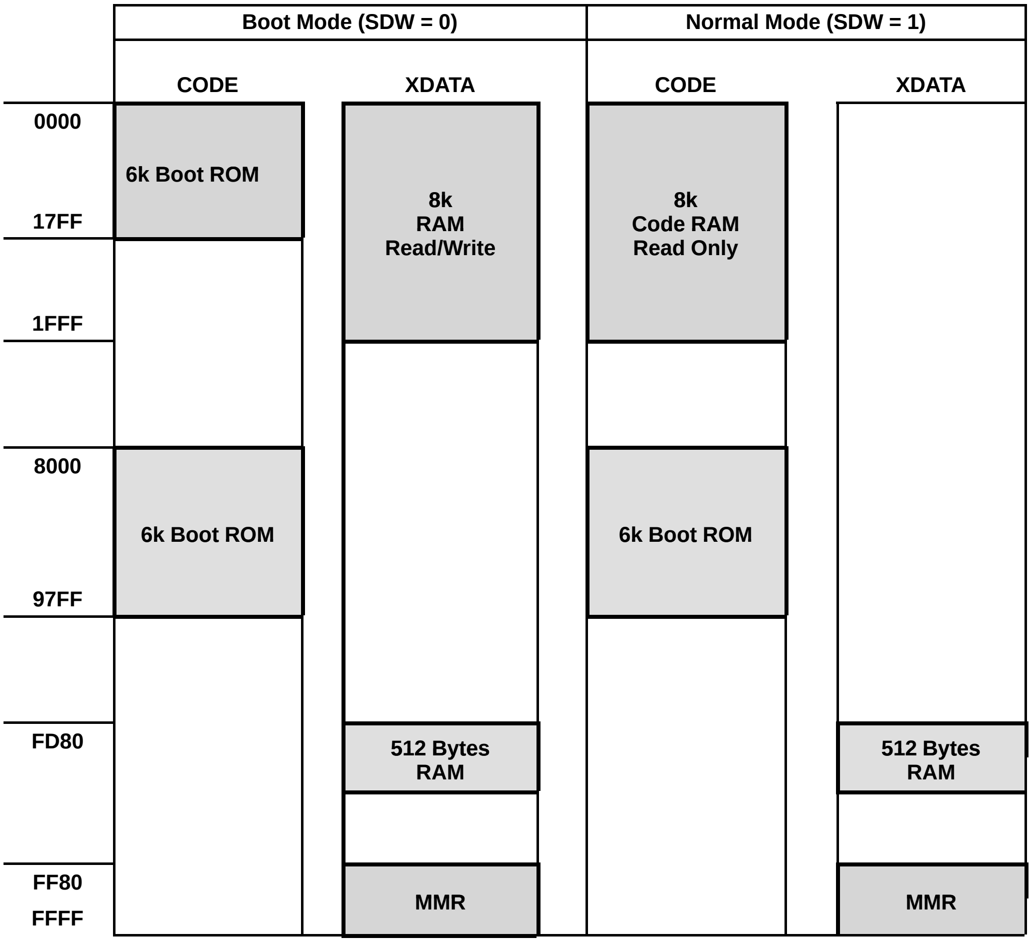


Figure 2–1. MCU Memory Map (TUSB2136B)

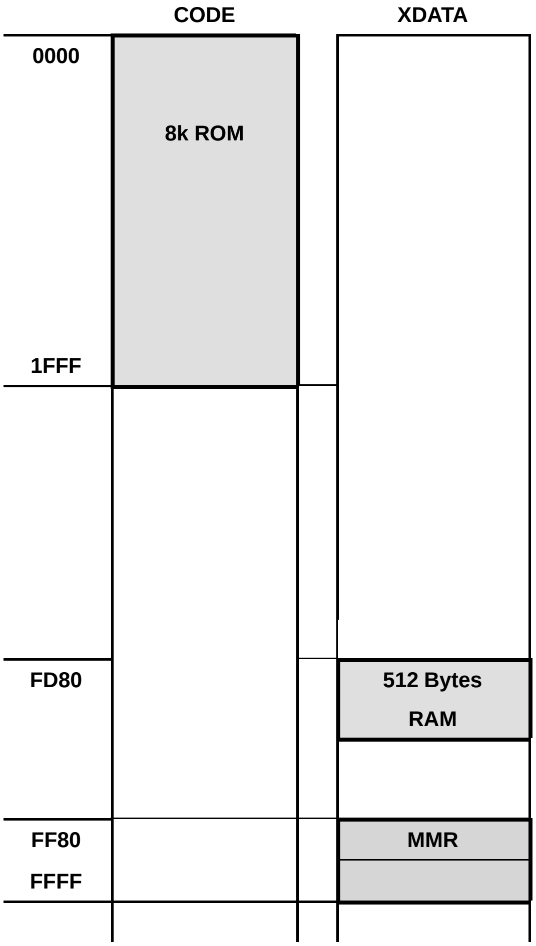


Figure 2–2. MCU Memory Map (ROM Version)

2.2 Miscellaneous Registers

2.2.1 TUSB2136 Boot Operation

Since the code-space is in RAM (with the exception of the boot ROM), the TUSB2136 firmware must be loaded from an external source. Two options for booting are available: an external serial EEPROM source connected to the I^{2}C bus, or the host may be used via the USB. On device reset, the SDW bit (in ROM register) and CONT bit in USB control register (USBCTL) is cleared. This configures the memory space to boot mode (see memory map) and keeps the device *disconnected* from the host.

The first instruction is fetched from location 0000 (which is in the 6k-ROM). The 8k-RAM is mapped to XDATA space (location 0000h). MCU executes a read from an external EEPROM and tests to see if it contains the code (test for boot signature). If it contains the code, MCU reads from EEPROM and writes to the 8k-RAM in XDATA space. If not, MCU proceeds to boot from USB.

Once the code is loaded, the MCU sets SDW to 1. This switches the memory map to normal mode, i.e. the 8k-RAM is mapped to code space, and the MCU starts executing from location 0000h. Once the switch is done, the MCU sets CONT to 1 (in USBCTL register) This *connects* the device to the USB bus, resulting in the normal USB device enumeration.

2.2.2 MCNFG: MCU Configuration Register

This register is used to control the MCU clock rate.

7	6	5	4	3	2	1	0
12/48	XINT	OVCE	R3	R2	R1	R0	SDW
R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/W

BIT	NAME	RESET	FUNCTION	
0	SDW	0	This bit enables/disables boot ROM. In the ROM version of the controller, this bit has no effect.	
			SDW = 0	When clear, MCU executes from the 6k boot ROM space. The boot ROM appears in two locations: 0000 and 8000h. The 8k RAM is mapped to XDATA space; therefore, Read/Write operation is possible. This bit is set by MCU after the RAM load is completed. MCU cannot clear this bit. It is cleared on power-up-reset or function reset.
			SDW = 1	When set by MCU, the 6k boot ROM maps to location 8000h, and the 8k RAM is mapped to code-space, starting at location 0000h. At this point, MCU executes from RAM, and write operation is disabled (No write operation is possible in code space).
4–1	R[3:0]	No affect	These bits reflect the device revision number	
5	OVCE	0	Hub overcorrect detection enable/disable bit. OVCE = 0 Hub overcorrect detection is disabled OVCE = 1 Hub overcorrect detection is enabled	
6	XINT	0	INT1 source control bit. XINT = 0 INT1 is connected to P3.3-pin and operates as a standard INT1 interrupt XINT = 1 INT1 is connected to the OR of Port–2 inputs.	
7	12/48	0	This bit selects 12 or 48 MHz clock for MCU 12/48 = 0 12 MHz 12/48 = 1 48 MHz	

2.2.3 PUR_n: GPIO Pullup Register for Port n (n = 0 to 3)

7	6	5	4	3	2	1	0
Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1	Pin0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
0–7	PinN (N = 0 to 7)	0	The MCU may write to this register. If the MCU sets this bit to 1, the pullup resistor is disconnected from the pin. If the MCU clears this bit to 0, the pullup resistor is connected to the pin. The pullup resistor is connected to V_{CC} power supply.

2.2.4 INTCFG: Interrupt Configuration

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	I3	I2	I1	I0
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
0–3	I[3:0]	0010	The MCU may write to this register to set the interrupt delay time for Port 2 on the MCU. The value of the lower nibble represents the delay in ms. Default after reset is 2 ms.
4–7	RSV	0	Reserved

2.2.5 WDCSR: Watchdog Timer, Control, and Status Register

A watchdog timer (WDT) with 1ms clock is provided. If this register is not accessed for a period of 32ms, the WDT counter resets the MCU. (See Figure 2–3, Reset Diagram). When the IDL bit in PCON is set, the WDT is suspended until an interrupt is detected. At this point, the IDL bit is cleared and the WDT resumes operation.

7	6	5	4	3	2	1	0
WDE	WDR	RSV	RSV	RSV	RSV	RSV	WDT
R/W	R/W	R/O	R/O	R/O	R/O	R/O	W/O

BIT	NAME	RESET	FUNCTION	
0	WDT	0	MCU must write a 1 to this bit to prevent the WDT from resetting the MCU. If MCU does not write a 1 in a period of 31ms, the WDT will reset the device. Writing a 0 has no effect on the WDT. (WDT is a 5-bit counter using 1ms CLK). This bit is read as 0.	
5–1	RSV	0	Reserved = 0	
6	WDR	0	Watchdog reset indication bit. This bit indicates if the reset occurred due to power-on reset or watchdog timer reset.	
			WDR = 0	A power-up or USB reset occurred.
			WDR = 1	A watchdog timeout reset occurred. To clear this bit, the MCU must write a 1. Writing a 0 has no effect.
7	WDE	0	Watchdog Timer Enable.	
			WDE = 0	This bit is cleared only on power-up, USB-reset (if enabled) or WDT reset.
			WDE = 1	When MCU writes a 1 to this bit the WDT will start running. MCU cannot disable the WDT. Only power up or USB reset (if enabled) can clear it. When MCU is in idle state (IDL = 1), the WDT is suspended.

2.2.6 PCON: Power Control Register (at SFR 87h)

7	6	5	4	3	2	1	0
SMOD	RSV	RSV	RSV	GF1	GF0	RSV	IDL
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/W

BIT	NAME	RESET	FUNCTION	
0	IDL	0	MCU idle mode bit. This bit can be set by MCU and is cleared only by $\overline{\text{INT1}}$ interrupt.	
			IDL = 0	MCU is NOT in idle mode. This bit is cleared by $\overline{\text{INT1}}$ interrupt logic when $\overline{\text{INT1}}$ is asserted for at least 400µs.
			IDL = 1	MCU is in idle mode and RAM is in low-power mode. The oscillator/APLL is off and the WDT will be suspended. When in suspend mode, only $\overline{\text{INT1}}$ can be used to exit from idle mode and generate an interrupt. $\overline{\text{INT1}}$ must be asserted for at least 400µs for the interrupt to be recognized.
1	RSV	0	Reserved = 0	
3–2	GF[1:0]	00	General-purpose bits. MCU can write and read them.	
6–4	RSV	0	Reserved = 0	
7	SMOD	0	Double baud rate control bit. For more information see UART serial interface in M8052 core specification.	

2.3 Buffers + I/O RAM Map

The address range from FD80 to FFFF is reserved for data buffers, setup packet, endpoint descriptor blocks (EDB), and all I/O. RAM space of 512 bytes [FD80–FF7F] is used for EDB and buffers. The FF80–FFFF range is used for memory mapped registers (MMR). Table 2–1 represents the internal XDATA space allocation.

Table 2–1. XDATA Space

DESCRIPTION	ADDRESS RANGE	
Internal MMR (Memory mapped registers)	FFFF ↑ FF80	
EDB (Endpoint descriptor blocks)	FF7F ↑ FF08	**512 byte RAM**
Setup packet buffer	FF07 ↑ FF00	
Input endpoint-0 buffer	FEFF ↑ FEF8	
Output endpoint-0 buffer	FEF7 ↑ FEF0	
Data buffers (367 bytes)	FEEF ↑ FD80	

Table 2–2. Memory Mapped Registers Summary (XDATA Range = FF80 → FFFF)

ADDRESS	REGISTER	DESCRIPTION
FFFF	FUNADR	FUNADR: Function address register
FFFE	USBSTA	USBSTA: USB status register
FFFD	USBMSK	USBMSK: USB interrupt mask register
FFFC	USBCTL	USBCTL: USB control register
FFFB	HUBVIDH	HUBVIDH: HUB-VID register (high-byte)
FFFA	HUBVIDL	HUBVIDL: HUB-VID register (low-byte)
FFF9	HUBPIDH	HUBPIDH: HUB-PID register (high-byte)
FFF8	HUBPIDL	HUBPIDL: HUB-PID register (low-byte)
FFF7	HUBCNFG	HUBCNFG: HUB-configuration register
FFF6	VIDSTA	VIDSTA: VID/PID status register
FFF5	HUBPOTG	HUBPOTG: HUB power-on to power-good descriptor register
FFF4	HUBCURT	HUBCURT: HUB current descriptor register
FFF3	I2CADR	I2CADR: I2C address register
FFF2	I2CDAI	I2CDAI: I2C data-input register
FFF1	I2CDAO	I2CDAO: I2C data-output register
FFF0	I2CSTA	I2CSTA: I2C status and control register
↑	RESERVED	
FF97	PUR3	Port 3 pullup resistor register

Table 2–2. Memory Mapped Registers Summary (XDATA Range = FF80 → FFFF) (Continued)

ADDRESS	REGISTER	DESCRIPTION
FF96	PUR2	Port 2 pullup resistor register
FF95	PUR1	Port 1 pullup resistor register
FF94	PUR0	Port 0 pullup resistor register
FF93	WDCSR	WDCSR: Watchdog timer, control & status register
FF92	VECINT	VECINT: Vector interrupt register
FF91	RESERVED	
FF90	MCNFG	MCNFG: MCU configuration register
↑	RESERVED	
FF84	INTCFG	INTCFG: Interrupt delay configuration register
FF83	OEPBCNT_0	OEPBCNT_0: Output endpoint-0 byte count register
FF82	OEPCNFG_0	OEPCNFG_0: Output endpoint-0 configuration register
FF81	IEPBCNT_0	IEPBCNT_0: Input endpoint-0 byte count register
FF80	IEPCNFG_0	IEPCNFG_0: Input endpoint-0 configuration register

Table 2–3. EDB and Buffers Allocations in XDATA

ADDRESS		DESCRIPTION
FF7F ↑ FF60	(32–bytes)	RESERVED
FF5F ↑ FF58	(8–bytes)	Input endpoint_3: configuration
FF57 ↑ FF50	(8–bytes)	Input endpoint_2: configuration
FF4F ↑ FF48	(8–bytes)	Input endpoint_1: configuration
FF47 ↑ FF20	(40–bytes)	RESERVED
FF1F ↑ FF18	(8–bytes)	Output endpoint_3: configuration
FF17 ↑ FF10	(8–bytes)	Output endpoint_2: configuration
FF0F ↑ FF08	(8–bytes)	Output endpoint_1: configuration

Table 2–3. EDB and Buffers Allocations in XDATA (Continued)

ADDRESS		DESCRIPTION
FF07 ↑ FF00	(8–bytes)	Setup packet block
FEFF ↑ FEF8	(8–bytes)	Input endpoint–0 buffer
FEF7 ↑ FEF0	(8–bytes)	Output endpoint–0 buffer
FEEF	TOPBUFF	Top of buffer space
↑ │ │		Buffers space
FD80	STABUFF	Start of buffer space

2.4 Endpoint Descriptor Block (EDB-1 to EDB-3)

Data transfers between USB, MCU and external devices are defined by an endpoint descriptor block (EDB). Four input and four output EDBs are provided. With the exception of EDB-0 (I/O Endpoint-0), all EDBs are located in SRAM as shown in Table 2–3. Each EDB contains information describing the X and Y buffers. In addition, it provides general status information.

Table 2–4 illustrates the EDB entries for EDB–1 to EDB–3. EDB–0 registers will be described separately.

Table 2–4. EDB Entries in RAM (n = 1 to 3)

Offset	ENTRY NAME	DESCRIPTION
07	EPSIZXY_n	I/O endpoint_n: X/Y buffer size
06	EPBCTY_n	I/O endpoint_n: Y byte count
05	EPBBAY_n	I/O endpoint_n: Y buffer base address
04	SPARE	Not used
03	SPARE	Not used
02	EPBCTX_n	I/O endpoint_n: X byte count
01	EPBBAX_n	I/O endpoint_n: X buffer base address
00	EPCNF_n	I/O endpoint_n: configuration

2.4.1 OEPCNF_n: Output Endpoint Configuration (n=1 to 3)

7	6	5	4	3	2	1	0
UBME	ISO	TOGLE	DBUF	STALL	USBIE	RSV	RSV
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/O

BIT	NAME	RESET	FUNCTION	
1–0	RSV	x	Reserved = 0	
2	USBIE	x	USB interrupt enable on transaction completion. Set/clear by MCU. USBIE = 0 no interrupt USBIE = 1 interrupt on transaction completion	
3	STALL	0	USB stall condition indication. Set/clear by MCU.	
			STALL = 0	No stall
			STALL = 1	USB stall condition. If set by MCU, a STALL handshake is initiated and the bit is cleared by MCU.
4	DBUF	x	Double buffer enable. Set/clear by MCU.	
			DBUF = 0	Primary buffer only (X–buffer only)
			DBUF = 1	Toggle bit selects buffer
5	TOGLE	x	USB Toggle bit. This bit reflects the toggle sequence bit of DATA0, DATA1	
6	ISO	x	ISO = 0	Non-isochronous transfer. This bit must be cleared by MCU since only non-isochronous transfer is supported.
7	UBME	x	UBM enable/disable bit. Set/clear by MCU. UBME = 0 UBM cannot use this endpoint. UBME = 1 UBM can use this endpoint.	

2.4.2 OEPBBAX_n: Output Endpoint X-Buffer Base-Address (n=1 to 3)

7	6	5	4	3	2	1	0
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	A[10:3]	x	A[10:3] of X–buffer base address (padded with 3-LSB of zeros for a total of 11-bits). This value is set by the MCU. UBM or DMA uses this value as the start-address of a given transaction. Furthermore, UBM or DMA does not change this value at the end of a transaction.

2.4.3 OEPBCTX_n: Output Endpoint X Byte Count (n=1 to 3)

7	6	5	4	3	2	1	0
NAK	C_6	C_5	C_4	C_3	C_2	C_1	C_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	C[6:0]	x	**X-Buffer Byte count:** X000.0000b > Count = 0 X000.0001b > Count = 1 byte : : X011.1111b > Count = 63 bytes X100.0000b > Count = 64 bytes Any value ≥ 100.0001b produces unpredictable results.
7	NAK	x	NAK= 0 No valid data in buffer. Ready for host out NAK= 1 Buffer contains a valid packet from Host (host-out request is NAK)

2.4.4 OEPBBAY_n: Output Endpoint Y-Buffer Base-Address (n=1 to 3)

7	6	5	4	3	2	1	0
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	A[10:3]	x	A[10:3] of Y–buffer base address (padded with 3-LSB of zeros for a total of 11 bits). This value is set by the MCU. UBM or DMA uses this value as the start-address of a given transaction. Furthermore, UBM or DMA does not change this value at the end of a transaction.

2.4.5 OEPBCTY_n: Output Endpoint Y Byte Count (n=1 to 3)

7	6	5	4	3	2	1	0
NAK	C_6	C_5	C_4	C_3	C_2	C_1	C_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	C[6:0]	x	**Y-Byte count:** X000.0000b > Count = 0 X000.0001b > Count = 1 byte : : X011.1111b > Count = 63 bytes X100.0000b > Count = 64 bytes Any value ≥ 100.0001b will result in unpredictable results.
7	NAK	x	NAK= 0 No valid data in buffer. Ready for host out NAK= 1 Buffer contains a valid packet from host (host-out request is NAK)

2.4.6 OEPSIZXY_n: Output Endpoint X/Y Byte Count (n=1 to 3)

7	6	5	4	3	2	1	0
RSV	S_6	S_5	S_4	S_3	S_2	S_1	S_0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	S[6:0]	x	**X AND Y-Buffer size:** 0000.0000b > Count = 0 0000.0001b > Count = 1 byte : : 0011.1111b > Count = 63 bytes 0100.0000b > Count = 64 bytes Any value ≥ 100.0001b produces unpredictable results.
7	RSV	x	Reserved = 0

2.4.7 IEPCNF_n: Input Endpoint Configuration (n=1 to 3)

7	6	5	4	3	2	1	0
UBME	ISO	TOGLE	DBUF	STALL	USBIE	RSV	RSV
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/O

BIT	NAME	RESET	FUNCTION
1–0	RSV	x	Reserved = 0
2	USBIE	x	USB interrupt enable on transaction completion. USBIE = 0 No interrupt USBIE = 1 Interrupt on transaction completion
3	STALL	0	USB stall condition indication. Set by UBM, but can be set/cleared by MCU. STALL = 0 No stall STALL = 1 USB stall condition. If set by MCU, a STALL handshake will be initiated and the bit is cleared automaticallly.
4	DBUF	x	Double buffer enable DBUF = 0 Primary buffer only (X–buffer only) DBUF = 1 Toggle bit selects buffer
5	TOGLE	x	USB Toggle bit. This bit reflects the toggle sequence bit of DATA0, DATA1
6	ISO	x	ISO = 0 Non-isochronous transfer. This bit must be cleared by MCU since only non-isochronous transfer is supported.
7	UBME	x	UBM enable/disable bit. Set/clear by MCU. UBME = 0 UBM cannot use this endpoint. UBME = 1 UBM can use this endpoint.

2.4.8 IEPBBAX_n: Input Endpoint X-Buffer Base-Address (n=1 to 3)

7	6	5	4	3	2	1	0
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	A[10:3]	x	A[10:3] of X-buffer base address (padded with 3-LSB of zeros for a total of 11 bits). This value is set by the MCU. UBM or DMA uses this value as the start-address of a given transaction. Furthermore, UBM or DMA does not change this value at the end of a transaction.

2.4.9 IEPBCTX_n: Input Endpoint X-Byte Base-Address (n=1 to 3)

7	6	5	4	3	2	1	0
NAK	C_6	C_5	C_4	C_3	C_2	C_1	C_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	C[6:0]	x	**X-Buffer Byte count:** X000.0000b > Count = 0 X000.0001b > Count = 1 byte : : X011.1111b > Count = 63 bytes X100.0000b > Count = 64 bytes Any value ≥ 100.0001b produces unpredictable results.
7	NAK	x	NAK = 0 Buffer contains a valid packet for host-in transaction NAK = 1 Buffer is empty (host-in request is NAK)

2.4.10 IEPBBAY_n: Input Endpoint Y-Buffer Base-Address (n=1 to 3)

7	6	5	4	3	2	1	0
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	A[10:3]	x	A[10:3] of Y-buffer base address (padded with 3-LSB of zeros for a total of 11 bits). This value is set by the MCU. UBM or DMA uses this value as the start-address of a given transaction. Furthermore, UBM or DMA does not change this value at the end of a transaction.

2.4.11 IEPBCTY_n: Input Endpoint Y Byte Count (n=1 to 3)

7	6	5	4	3	2	1	0
NAK	C_6	C_5	C_4	C_3	C_2	C_1	C_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	C[6:0]	x	**X-Byte count:** X000.0000b > Count = 0 X000.0001b > Count = 1 byte : : X011.1111b > Count = 63 bytes X100.0000b > Count = 64 bytes Any value ≥ 100.0001b produces unpredictable results.
7	NAK	x	NAK = 0 Buffer contains a valid packet for host-in transaction NAK = 1 Buffer is empty (host-in request is NAK)

2.4.12 IEPSIZXY_n: Input Endpoint X/Y-Buffer Size (n=1 to 3)

7	6	5	4	3	2	1	0
RSV	S_6	S_5	S_4	S_3	S_2	S_1	S_0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	S[6:0]	x	**X AND Y-Buffer size:** 0000.0000b > Count = 0 0000.0001b > Count = 1 byte : : 0011.1111b > Count = 63 bytes 0100.0000b > Count = 64 bytes Any value ≥ 100.0001b produces unpredictable results.
7	RSV	x	Reserved = 0

2.5 Endpoint-0 Descriptor Registers

Unlike EDB-1 to EDB-3, which are defined as memory entries in SRAM, Endpoint-0 is described by a set of 4 registers (two for output and two for input). Table 2–5 defines the registers and their respective addresses used for EDB-0 description. EDB-0 has no *Base-Address-Register*, since these addresses are hardwired to FEF8 and FEF0. Note that the bit positions have been preserved to provide consistency with EDB-n (n = 1 to 3).

Table 2–5. Input/Output EDB-0 Registers

ADDRESS	REGISTER NAME	DESCRIPTION	BASE ADDRESS
FF83	OEPBCNT_0	Output endpoint–0: byte count register	FEF0
FF82	OEPCNFG_0	Output endpoint–0: configuration register	
FF81	IEPBCNT_0	Input endpoint–0: byte count register	FEF8
FF80	IEPCNFG_0	Input endpoint–0: configuration register	

2.5.1 IEPCNFG_0: Input Endpoint-0 Configuration Register

7	6	5	4	3	2	1	0
UBME	RSV	TOGLE	RSV	STALL	USBIE	RSV	RSV
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O

BIT	NAME	RESET	FUNCTION
1–0	RSV	0	Reserved = 0
2	USBIE	0	USB interrupt enable on transaction completion. Set/clear by MCU USBIE = 0 No interrupt USBIE = 1 Interrupt on transaction completion
3	STALL	0	USB stall condition indication. Set/clear by MCU. STALL = 0 No stall STALL = 1 USB stall condition. If set by MCU, a STALL handshake is initiated and the bit is cleared automaticallly by next setup transaction.
4	RSV	0	Reserved = 0
5	TOGLE	0	USB toggle bit. This bit reflects the toggle sequence bit of DATA0, DATA1
6	RSV	0	Reserved = 0
7	UBME	0	UBM enable/disable bit. Set/clear by MCU. UBME = 0 UBM cannot use this endpoint. UBME = 1 UBM can use this endpoint.

2.5.2 IEPBCNT_0: Input Endpoint-0 Byte Count Register

7	6	5	4	3	2	1	0
NAK	RSV	RSV	RSV	C_3	C_2	C_1	C_0
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
3–0	C[3:0]	0000	**Byte count:** 0000b > Count = 0 : : 0111b > Count =7 1000b > Count = 8 1001b to 1111b are reserved. (If used, defaults to 8)
6–4	RSV	0	Reserved = 0
7	NAK	1	NAK= 0 Buffer contains a valid packet for host-in transaction NAK= 1 Buffer is empty (host-in request is NAK)

2.5.3 OEPCNFG_0: Output Endpoint-0 Configuration Register

7	6	5	4	3	2	1	0
UBME	RSV	TOGLE	RSV	STALL	USBIE	RSV	RSV
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O

BIT	NAME	RESET	FUNCTION	
1–0	RSV	0	Reserved = 0	
2	USBIE	0	USB interrupt enable on transaction completion. Set/clear by MCU USBIE = 0 no interrupt USBIE = 1 interrupt on transaction completion	
3	STALL	0	USB stall condition indication. Set/clear by MCU.	
			STALL = 0	No stall
			STALL = 1	USB stall condition. If set by MCU, a STALL handshake is initiated and the bit is cleared automaticallly.
4	RSV	0	Reserved = 0	
5	TOGLE	0	USB toggle bit. This bit reflects the toggle sequence bit of DATA0, DATA1	
6	RSV	0	Reserved = 0	
7	UBME	0	UBM enable/disable bit. Set/clear by MCU. UBME = 0 UBM cannot use this endpoint. UBME = 1 UBM can use this endpoint.	

2.5.4 OEPBCNT_0: Output Endpoint-0 Byte Count Register

7	6	5	4	3	2	1	0
NAK	RSV	RSV	RSV	C_3	C_2	C_1	C_0
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
3–0	C[3:0]	0000	**Byte count:** 0000b > Count = 0 : : 0111b > Count =7 1000b > Count = 8 1001b to 1111b are reserved. (If used, defaults to 8)
6–4	RSV	0	Reserved = 0
7	NAK	1	NAK= 0 No valid data in buffer. Ready for host out NAK= 1 Buffer contains a valid packet from host. (NAK the host)

2.6 USB Registers

2.6.1 FUNADR: Function Address Register

This register contains the device function address.

7	6	5	4	3	2	1	0
RSV	FA6	FA5	FA4	FA3	FA2	FA1	FA0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
6–0	FA[6:0]	0000000	These bits define the current device address assigned to the function. MCU writes a value to this register as a result of *SET-ADDRESS* host command.
7	RSV	0	Reserved = 0

2.6.2 USBSTA: USB Status Register

All bits in this register are set by the hardware and will be cleared by MCU when writing a 1 to the proper bit location (writing a 0 has no effect). In addition, each bit can generate an interrupt if its corresponding mask bit is set (R/C notation indicates read and clear only by MCU).

7	6	5	4	3	2	1	0
RSTR	SUSR	RESR	PWOFF	PWON	SETUP	RSV	STPOW
R/C	R/C	R/C	R/C	R/C	R/C	R/O	R/C

BIT	NAME	RESET	FUNCTION	
0	STPOW	0	SETUP overwrite bit. Set by hardware when setup packet is received while there is already a packet in the setup buffer.	
			STPOW = 0	MCU can clear this bit by writing a 1. (Writing 0 has no effect)
			STPOW = 1	SETUP overwrite
1	RSV	0	Reserved = 0	
2	SETUP	0	SETUP transaction received bit. As long as SETUP is 1, IN and OUT on endpoint-0 is NAK regardless of the value of their real NAK bits.	
			SETUP = 0	MCU can clear this bit by writing a 1. (Writing 0 has no effect)
			SETUP = 1	SETUP transaction received.
3	PWON	0	Power on request for Port-3. This bit indicates if power-on to Port-3 has been received. This bit generates a PWON interrupt (If enabled).	
			PWON = 0	MCU can clear this bit by writing a 1. (Writing 0 has no effect)
			PWON = 1	Power on to Port-3 has been received.
4	PWOFF	0	Power off request for Port-3. This bit indicates whether power-off to Port-3 has been received. This bit generates a PWOFF interrupt (If enabled).	
			PWOFF = 0	MCU can clear this bit by writing a 1. (Writing 0 has no effect)
			PWOFF = 1	Power off to Port-3 has been received
5	RESR	0	Function resume request bit	
			RESR = 0	MCU can clear this bit by writing a 1. (Writing 0 has no effect)
			RESR = 1	Function resume is detected
6	SUSR	0	Function suspended request bit. This bit is set in response to a global or selective suspend condition. SUSR =0 MCU can clear this bit by writing a 1. (Writing 0 has no effect) SUSR =1 Function suspend is detected.	
7	RSTR	0	Function reset request bit. This bit is set in response to host initiating a port reset. This bit is not affected by USB function reset. RSTR = 0 MCU can clear this bit by writing a 1. (Writing 0 has no effect) RSTR = 1 Function reset is detected.	

2.6.3 USBMSK: USB Interrupt Mask Register

7	6	5	4	3	2	1	0
RSTR	SUSR	RESR	PWOFF	PWON	SETUP	RSV	STPOW
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W

BIT	NAME	RESET	FUNCTION
0	STPOW	0	SETUP overwrite interrupt enable bit STPOW = 0 STPOW interrupt disabled STPOW = 1 STPOW interrupt enabled
1	RSV	0	Reserved = 0
2	SETUP	0	SETUP interrupt enable bit SETUP = 0 SETUP interrupt disabled SETUP = 1 SETUP interrupt enabled
3	PWON	0	Power-on interrupt enable bit PWON = 0 PWON interrupt disabled PWON = 1 PWON interrupt enabled
4	PWOFF	0	Power-off interrupt enable bit PWOFF = 0 PWOFF interrupt disabled PWON = 1 PWOFF interrupt enabled
5	RESR	0	Function resume interrupt enable RESR = 0 function resume interrupt disabled RESR = 1 function resume interrupt enabled
6	SUSR	0	Function suspend interrupt enable SUSR = 0 function suspend interrupt disabled SUSR = 1 function suspend interrupt enabled
7	RSTR	0	Function reset interrupt enable RSTR = 0 function reset interrupt disabled RSTR = 1 function reset interrupt enabled

2.6.4 USBCTL: USB Control Register

Unlike the other registers, this register is cleared by the power-up-reset signal only. The USB-reset cannot reset this register. (See Figure 2–3: Reset Diagram)

7	6	5	4	3	2	1	0
CONT	U1/2	RWUP	FRSTE	RWE	B/S	SIR	DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<table>
<tr><th>BIT</th><th>NAME</th><th>RESET</th><th colspan="2">FUNCTION</th></tr>
<tr><td>0</td><td>DIR</td><td>0</td><td colspan="2">As a response to a setup packet, the MCU will decode the request and set or clear this bit to reflect the data transfer direction.
DIR = 0 > USB data OUT transaction. (From host to TUSB2136)
DIR = 1 > USB data IN transaction. (From TUSB2136 to host)</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">SIR</td><td rowspan="3">0</td><td colspan="2">SETUP interrupt status bit. This bit is controlled by the MCU to indicate to the hardware when SETUP interrupt is being served.</td></tr>
<tr><td>SIR = 0</td><td>SETUP interrupt is not served. MCU will clear this bit before exiting the SETUP interrupt routine.</td></tr>
<tr><td>SIR = 1</td><td>SETUP interrupt is in progress. MCU will set this bit when servicing the SETUP interrupt.</td></tr>
<tr><td>2</td><td>B/S</td><td>0</td><td colspan="2">Bus/self power control bit
B/S = 0 > The device is bus-powered
B/S = 1 > The device is self-powered</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">RWE</td><td rowspan="3">0</td><td colspan="2">Remote wake-up enable bit.</td></tr>
<tr><td>RWE = 0</td><td>MCU clears it when host sends command to clear the feature.</td></tr>
<tr><td>RWE = 1</td><td>MCU writes 1 to it when host sends *set device feature command* to enable remote wake-up feature</td></tr>
<tr><td>4</td><td>FRSTE</td><td>1</td><td colspan="2">Function reset connection bit. This bit connects/disconnects the USB function reset from the MCU reset.
FRSTE = 0 function reset is not connected to MCU reset
FRSTE = 1 function reset is connected to MCU reset</td></tr>
<tr><td rowspan="3">5</td><td rowspan="3">RWUP</td><td rowspan="3">0</td><td colspan="2">Device remote wake-up request. This bit is set by MCU and is cleared automatically.</td></tr>
<tr><td>RWUP = 0</td><td>Writing a 0 to this bit has no effect.</td></tr>
<tr><td>RWUP = 1</td><td>When MCU writes a 1, a Remote wake-up pulse is generated.</td></tr>
<tr><td>6</td><td>U1/2</td><td>0</td><td colspan="2">USB hub version
U1/2 = 0 > This is a USB1.x Hub
U1/2 = 1 > This is a USB2.x Hub</td></tr>
<tr><td>7</td><td>CONT</td><td>0</td><td colspan="2">Connect/disconnect bit
CONT = 0 Upstream port is disconnected. Pullup disabled
CONT = 1 Upstream port is connected. Pullup enabled</td></tr>
</table>

2.6.5 HUBCNFG: HUB-Configuration Register

7	6	5	4	3	2	1	0
OCP	I/G	P3.1	P3.0	P2A	P2E	P1A	P1E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
0	P1E	0	Hub Port-1; enable/disable control bit. P1E = 0 > Port-1 is disabled. P1E = 1 > Port-1 Is enabled
1	P1A	0	Hub Port–1; permanent attachment control bit. P1A = 0 > Port-1 is connected to a removable function. P1A = 1 > Port-1 is connected to a permanent attachment function.
2	P2E	0	Hub Port-2; enable/disable control bit. P2E = 0 > Port-2 is disabled. P2E = 1 > Port-2 Is enabled
3	P2A	0	Hub Port-2; permanent attachment control bit. P2A = 0 > Port-2 is connected to a removable function. P2A = 1 > Port-2 is connected to a permanent attachment function.
5–4	P3[1:0]	00	Hub Port-3; embedded function control field. 00b = Port-3 is disabled (doesn't exist). 01b = Port-3 is permanently attached 10b = Port-3 is connected to a removable function, but is not attached 11b = Port-3 is connected to a removable function, and is attached
6	I/G	0	Individual/gang power control bit I/G = 0 > Overcurrent and power control are controlled individually I/G = 1 > Overcurrent and power control are gang controlled
7	OCP	0	Over current protection control bit OCP = 0 > Overcurrent protection is disabled OCP = 1 > Overcurrent protection is enabled

2.6.6 HUBPOTG: HUB Power-On to Power-Good Descriptor Register

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[7:0]	00h	Offset-5 in hub descriptor table

2.6.7 HUBCURT: HUB Current Descriptor Register

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[7:0]	00h	Offset-6 in hub descriptor table

2.6.8 HUBPIDL: HUB-PID Register (Low-Byte)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[7:0]	00h	Hub PID low byte value

2.6.9 HUBPIDH: HUB-PID Register (High-Byte)

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[15:8]	00h	Hub PID high byte value

2.6.10 HUBVIDL: HUB-VID Register (Low-Byte)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[7:0]	00h	Hub VID low byte value

2.6.11 HUBVIDH: HUB-VID Register (High-Byte)

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[15:8]	00h	Hub VID high byte value

2.6.12 VIDSTA: VID/PID Status Register

This register is used to read the value on four external pins. The firmware can use this value to select one of the vendor identification/product identifications (VID/PID) stored in memory. The TUSB2136/D supports up to 16 unique VID/PIDs with application code to support different products. This provides a unique opportunity for original equipment manufacturers (OEM) to have one device ROM programmed to support up to 16 different product lines by using S0–S3 to select VID/PID and behavioral application code for the selected product.

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	S3	S2	S1	S0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O

BIT	NAME	RESET	FUNCTION
3–0	S[3:0]	x	VID/PID selection bits. These bits reflect the status of the external pins as defined by Table 2–7. Note that a pin tied low will be reflected as 0 and a pin tied high will be reflected as a 1.
7–4	RSV	0	Reserved = 0

Table 2–6. External Pins Mapping to S[3:0] in VIDSTA Register

PIN		VIDSTA REGISTER	COMMENTS
NO.	NAME	S[3:0]	
58	P3.0	S0	Dual function P3.0 I/O or S0 input
57	P3.1	S1	Dual function P3.1 I/O or S1 input
8	S2	S2	S2-pin is input
9	S3	S3	S3-pin is input

2.7 Function Reset and Power-Up Reset Interconnect

Figure 2–3 represents the logical connection of USB-function-reset ($\overline{\text{USBR}}$) and power-up-reset ($\overline{\text{RST}}$-pin). The internal $\overline{\text{RESET}}$ signal is generated from the $\overline{\text{RST}}$ pin ($\overline{\text{PURS}}$ signal) or from the USB-reset ($\overline{\text{USBR}}$ signal). The $\overline{\text{USBR}}$ can be enabled or disabled by the FRSTE bit in the USBCTL register (on power up FRSTE is = 0). The internal $\overline{\text{RESET}}$ is used to reset all registers and logic, with the exception of the USBCTL and MISCTL registers. The USBCTL and MCU configuration register (MCNFG) are cleared by $\overline{\text{PURS}}$ signal only.

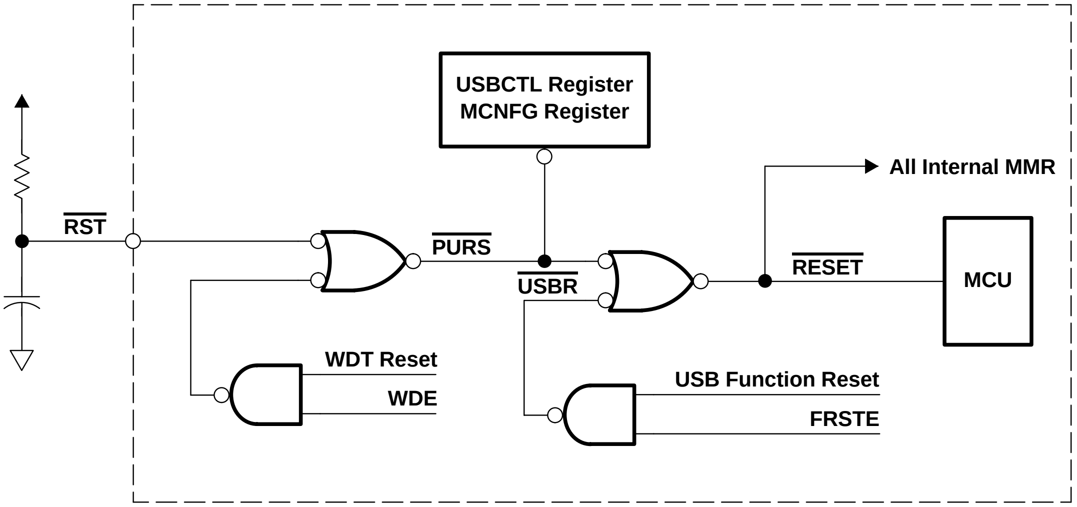


Figure 2–3. Reset Diagram

2.8 Pullup Resistor Connect/Disconnect

After reading firmware into RAM the TUSB2136 can re-enumerate using the new firmware (no need to physically disconnect and re-connect the cable). Figure 2–4 shows an equivalent circuit implementation for *Connect* and *Disconnect* from a USB upstream port (also see Firgure 4–4b). When CONT bit in USBCTL register is 1, the CMOS driver sources V_{DD} to the pullup resistor (PUR pin) presenting a normal connect condition to the USB hub (high speed). When CONT bit is 0, PUR pin is driven low. In this state, the 1.5-kΩ resistor is connected to GND, resulting in device *disconnection* state. The PUR driver is a CMOS driver that can provide (V_{DD}–0.1) volt minimum at 8 mA source current.

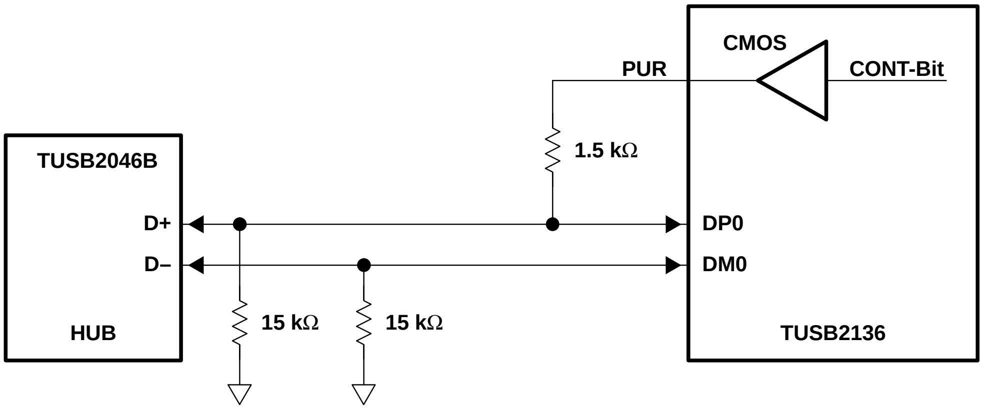


Figure 2–4. Pullup Resistor Connect/Disconnect Circuit

2.9 8052 Interrupt and Status Registers

All five standard interrupt sources of the 8052 are preserved. SIE is the standard interrupt enable register, which controls the five interrupt sources. All the additional interrupt sources are connected together as an OR to generate EX0. XINTO# signal is provided to interrupt an external MCU (see Interrupt connection diagram, Figure 2–5).

Table 2–7. 8052 Interrupt Location Map

INTERRUPT SOURCE	DESCRIPTION	START ADDRESS	COMMENTS
ES	UART interrupt	0023H	
ET1	Timer–1 interrupt	001BH	
EX1	Internal INT1	0013H	Used for P2[7:0] interrupt
ET0	Timer–0 interrupt	000BH	
EX0	Internal INT0	0003H	Used for all internal peripherals
Reset		0000H	

2.9.1 8052 Standard Interrupt Enable Register

7	6	5	4	3	2	1	0
EA	RSV	RSV	ES	ET1	EX1	ET0	EX0
R/W	R/O	R/O	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
0	EX0	0	Enable or disable external interrupt-0 EX0 = 0 external interrupt-0 is disabled EX0 = 1 external interrupt-0 is enabled
1	ET0	0	Enable or disable timer-0 interrupt ET0 = 0 timer-0 interrupt is disabled ET0 = 1 timer-0 interrupt is enabled
2	EX1	0	Enable or disable external interrupt-1 EX1 = 0 external interrupt-1 is disabled EX1 = 1 external interrupt-1 is enabled
3	ET1	0	Enable or disable timer-1 interrupt ET1 = 0 timer-1 interrupt is disabled ET1 = 1 timer-1 interrupt is enabled
4	ES	0	Enable or disable serial port interrupts ES = 0 serial port interrupt is disabled ES = 1 serial port interrupt is enabled
5,6	RSV	0	Reserved
7	EA	0	Enable or disable all interrupts (global disable) EA = 0 disable all interrupts EA = 1 each interrupt source is individually controlled.

2.9.2 Additional Interrupt Sources

All nonstandard 8052 interrupts (USB, I^2C, etc.) are connected as an OR to generate an internal INT0. It must be noted that the external INT0 and INT1 are not used. Furthermore, INT0 must be programmed as an active low level interrupt (not edge triggered). A vector interrupt register is provided to identify all interrupt sources (see vector interrupt register definition). Up to 64 interrupt vectors are provided. It is the responsibility of the MCU to read the vector and dispatch the proper interrupt routine.

2.9.3 VECINT: Vector Interrupt Register

This register contains a vector value identifying the internal interrupt source that trapped to location 0003H. Writing any value to this register removes the vector and update the next vector value (if another interrupt is pending). Note that the vector value is offset. Therefore, its value is in increments of two (bit-0 is set to 0). When no interrupt is pending, the vector is set to 00h. (see Table 2–8: Vector Interrupt Values). As shown, the interrupt vector is divided into two fields; I[2:0] and G[3:0]. The I-field defines the interrupt source within a group (on first come first served basis) and the G-field, which defines the group number. Group G0 is the lowest and G15 is the highest priority.

7	6	5	4	3	2	1	0
G3	G2	G1	G0	I2	I1	I0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/O

BIT	NAME	RESET	FUNCTION
3–1	I[2:0]	000	This field defines the interrupt source in a given group. See Table 2–8: Vector Interrupt Values. Bit-0 is always = 0, therefore, vector values will be offset by two.
7–4	G[3:0]	0000	This field defines the interrupt group. I[2:0] and G[3:0] combine to produce the actual interrupt vector.

Table 2–8. Vector Interrupt Values

G[3:0] (Hex)	I[2:0] (Hex)	VECTOR (Hex)	INTERRUPT SOURCE
0	0	00	No interrupt
1	0	10	NOT USED
1	1	12	Output endpoint-1
1	2	14	Output endpoint-2
1	3	16	Output endpoint-3
1	4–7	18–1E	NOT USED
2	0	20	NOT USED
2	1	22	Input endpoint-1
2	2	24	Input endpoint-2
2	3	26	Input endpoint-3
2	4–7	28–2E	NOT USED
3	0	30	STPOW packet received
3	1	32	SETUP packet received
3	2	34	PWON interrupt
3	3	36	PWOFF interrupt
3	4	38	RESR interrupt
3	5	3A	SUSR interrupt
3	6	3C	RSTR interrupt
3	7	3E	RESERVED
4	0	40	I2C TXE interrupt
4	1	42	I2C RXF interrupt
4	2	44	Input endpoint–0
4	3	46	Output endpoint–0
4	4–7	48 → 4E	NOT USED
5–15	X	90 → FE	NOT USED

2.9.4 Logical Interrupt Connection Diagram ($\overline{\text{INT0}}$)

Figure 2–5 represents the logical connection of the interrupt sources and its relation with XINTO#. The priority encoder generates an 8-bit vector, corresponding to 64 interrupt sources (not all are used). The interrupt priorities are hard wired. Vector 4E is the highest and 00 is the lowest.

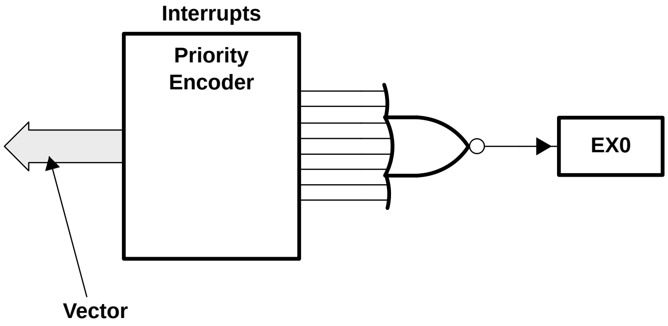


Figure 2–5. Internal Vector Interrupt (EX0)

2.9.5 P2[7:0] Interrupt ($\overline{\text{INT1}}$)

Figure 2–6 illustrates the conceptual Port-2 interrupt. All Port-2 input signals are connected in a logical OR to generate INT1 interrupt. Note that the inputs are active low and INT1 is programed as an edge-triggered interrupt. In addition, INT1 is connected to the suspend/resume logic for remote wake-up support. As illustrated, XINT-bit in MCU configuration register (MCNFG) is used to select the EXI interrupt source. When XINT = 0, P3.3 is the source, and when XINT = 1, P2[7:0] is the source.

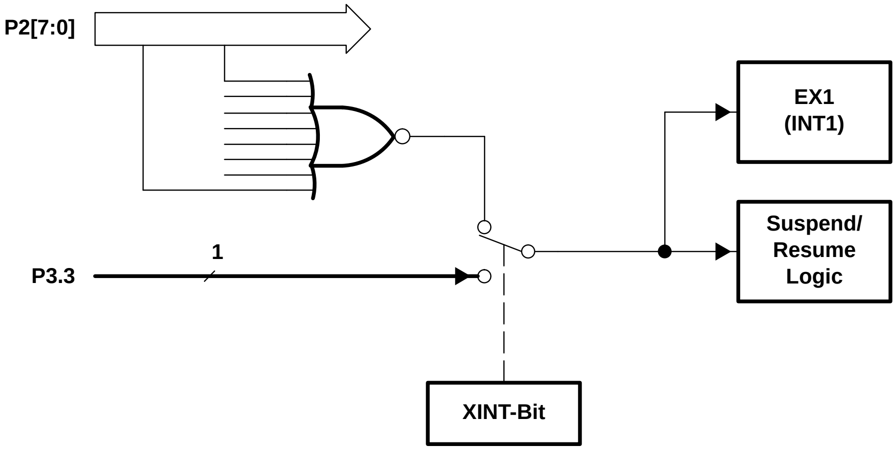


Figure 2–6. P2[7:0] Input Port Interrupt Generation

2.10 I2C Registers

2.10.1 I2CSTA: I2C Status and Control Register

This register is used to control the stop condition for read and write operation. In addition, it provides transmitter and receiver handshake signals with their respective interrupt enable bits.

7	6	5	4	3	2	1	0
RXF	RIE	ERR	1/4	TXE	TIE	SRD	SWR
R/C	R/W	R/C	R/W	R/C	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION	
0	SWR	0	Stop write condition. This bit defines if the I2C controller generates a stop condition when data from I2CDAO register is transmitted to an external device.	
			SWR = 0	Stop condition is not generated when data from I2CDAO register is shifted out to an external device.
			SWR = 1	Stop condition is generated when data from I2CDAO register is shifted out to an external device.
1	SRD	0	Stop read condition. This bit defines if the I2C controller will generate a stop condition when data is received and loaded into I2CDAI register.	
			SRD = 0	Stop condition is not generated when data from SDA line is shifted into I2CDAI register.
			SRD = 1	Stop condition is generated when data from SDA line is shifted into I2CDAI register.
2	TIE	0	I^{2}C transmitter empty interrupt enable. TIE = 0 Interrupt disable TIE = 1 Interrupt enable	
3	TXE	1	I^{2}C transmitter empty. This bit indicates that data can be written to the transmitter. It can be used for polling or it can generate an interrupt.	
			TXE = 0	Transmitter is full. This bit is cleared when MCU writes a byte to I2CDAO register.
			TXE = 1	Transmitter is empty. The I2C controller sets this bit when the content of I2CDAO register is copied to the SDA shift–register.
4	1/4	0	Bus speed selection. 1/4 = 0 > 100 kHz bus speed 1/4 = 1 > 400 kHz bus speed	
5	ERR	0	Bus error condition. This bit is set by the hardware when the device does not respond. It is cleared by the MCU. ERR = 0 No bus error ERR = 1 Bus error condition has been detected. Clears when MCU writes a 1. Writing a 0 has no effect.	
6	RIE	0	I^{2}C receiver ready interrupt enable. RIE = 0 Interrupt disable RIE = 1 Interrupt enable	
7	RXF	0	I^{2}C receiver full. This bit indicates that the receiver contains new data. It can be used for polling or it can generate an interrupt.	
			RXF = 0	Receiver is empty. This bit is cleared when MCU reads the I2CDAI register.
			RXF = 1	Receiver contains new data. This bit is set by the I2C controller when the received serial data has been loaded into I2CDAI register

2.10.2 I2CADR: I2C Address Register

This register holds the device address and the read/write command bit.

7	6	5	4	3	2	1	0
A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
0	R/W	0	Read/write command bit. R/W = 0 Write operation R/W = 1 Read operation
7–1	A[6:0]	0000000	Seven address bits for device addressing.

2.10.3 I2CDAI: I2C Data-Input Register

This register holds the received data from an external device.

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O

BIT	NAME	RESET	FUNCTION
7–0	D[7:0]	0	8-bit input data from an I2C device

2.10.4 I2CDAO: I2C Data-Output Register

This register holds the data to be transmitted to an external device. Writing to this register starts the transfer on the SDA line.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	RESET	FUNCTION
7–0	D[7:0]	0	8-bit output data to an I2C device

2.11 Read/Write Operations

2.11.1 Read Operation (Serial EEPROM)

A serial read requires a *dummy* byte write sequence to load in the 16-bit data word address. Once the device address word and data word address is clocked out and acknowledged by the device, the MCU starts a current address sequence. The following describes the sequence of events to accomplish this transaction:

Device Address + EEPROM [High-byte]

- MCU sets I2CSTA[SRD] = 0. This forces the I2C controller not to generate a stop condition after the content of I2CDAI register is received.
- MCU sets I2CSTA[SWR] = 0. This forces the I2C controller to NOT generate a stop condition after the content of I2CDAO register is transmitted.
- MCU writes the device address (R/W bit = 0) to I2CADR register (write operation)
- MCU writes the High-Byte of the EEPROM address into I2CDAO register, starting the transfer on SDA line
- TXE bit in I2CSTA is cleared, indicating busy

- The content of I2CADR register is transmitted to the EEPROM (preceded by start condition on SDA)
- The content of I2CDAO register is transmitted to the EEPROM (EEPROM address)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been transmitted
- No stop condition is generated

EEPROM [Low-byte]

- MCU writes the Low-byte of the EEPROM address into I2CDAO register
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CDAO register is transmitted to the device (EEPROM address)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been transmitted
- This completes the *dummy* write operation. At this point, the EEPROM address is set and the MCU can do a single or a sequential read operation.

2.11.2 Current Address Read Operation

Once the EEPROM address is set the MCU can read a single byte by executing the following steps:

1. MCU sets I2CSTA[SRD] = 1, forcing the I2C controller to generate a stop condition after I2CDAI register is received.
2. MCU writes the device address (R/W bit = 1) to I2CADR register (read operation).
3. MCU writes a dummy byte to I2CDAO register, starting the transfer on SDA line
4. RXF bit in I2CSTA is cleared
5. The content of I2CADR register is transmitted to the device, preceded by start condition on SDA
6. Data from the EEPROM is latched in I2CDAI register (stop condition is transmitted)
7. RXF bit in I2CSTA is set, and interrupt the MCU, indicating that the data is available.
8. MCU reads I2CDAI register. This clears RXF bit (I2CSTA[RXF] = 0)
9. END

2.11.3 Sequential Read Operation

Once the EEPROM address is set, the MCU can execute a sequential read operation by executing the following steps (Note: this example illustrates 32-byte sequential read):

1. Device Address
    - MCU sets I2CSTA[SRD] = 0. This forces the I2C controller to not generate a stop condition after I2CDAI register is received
    - MCU writes the device address (R/W bit = 1) to I2CADR register (read operation)
    - MCU writes a dummy byte to I2CDAO register, starting the transfer on SDA line
    - RXF bit in I2CSTA is cleared
    - The content of I2CADR register is transmitted to the device (preceded by start condition on SDA)
2. N-Byte Read (31-bytes)
    - Data from the device is latched in I2CDAI register (stop condition is not transmitted)
    - RXF bit in I2CSTA is set, and interrupt the MCU, indicating that data is available

- MCU reads I2CDAI register, clearing RXF bit (I2CSTA[RXF] = 0)
- This operation repeats 31 times

3. Last-Byte read (byte No. 32)
    - MCU sets I2CSTA[SRD] = 1. This forces the I2C controller to generate a stop condition after I2CDAI register is received
    - Data from the device is latched in I2CDAI register (Stop condition is transmitted)
    - RXF bit in I2CSTA is set, and interrupt the MCU, indicating that data is available
    - MCU reads I2CDAI register, clearing RXF bit (I2CSTA[RXF] = 0)
    - END

2.11.4 Write Operation (Serial EEPROM)

Byte write operation involves three phases: 1) device address + EEPROM [High–byte] phase, 2) EEPROM [Low–byte] phase, and 3) EEPROM [DATA]. The following describes the sequence of events to accomplish the byte write transaction:

Device Address + EEPROM [High-byte]

- MCU sets I2CSTA[SWR] = 0. This forces the I2C controller to not generate a stop condition after the content of I2CDAO register is transmitted.
- MCU writes the device address (R/W bit = 0) to I2CADR register (write operation)
- MCU writes the high-byte of the EEPROM address into I2CDAO register, starting the transfer on SDA line
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CADR register is transmitted to the device (preceded by start condition on SDA)
- The content of I2CDAO register is transmitted to the device (EEPROM high-address)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been transmitted

EEPROM [Low-byte]

- MCU writes the low–byte of the EEPROM address into I2CDAO register
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CDAO register is transmitted to the device (EEPROM address)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been transmitted

EEPROM [DATA]

- MCU sets I2CSTA[SWR] = 1. This forces the I2C controller to generate a stop condition after the content of I2CDAO register is transmitted.
- MCU writes the DATA to be written to the EEPROM into I2CDAO register
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CDAO register is transmitted to the device (EEPROM data)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been transmitted
- I2C controller generates a stop condition after the content of I2CDAO register is transmitted
- END

2.11.5 Page Write Operation

Page write operation is initiated the same way as byte write, with the exception that stop condition is not generated after the first EEPROM [DATA] is transmitted. The following describes the sequence of writing 32-bytes in page mode:

Device Address + EEPROM [High-byte]

- MCU sets I2CSTA[SWR] = 0. This forces the I2C controller to not generate a stop condition after the content of I2CDAO register is transmitted.
- MCU writes the device address (R/W bit = 0) to I2CADR register (write operation)
- MCU writes the high-byte of the EEPROM address into I2CDAO register.
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CADR register is transmitted to the device (preceded by start condition on SDA)
- The content of I2CDAO register is transmitted to the device (EEPROM address)
- TXE bit in I2CSTA is set, and interrupt the MCU, indicating that I2CDAO register has been sent.

EEPROM [Low-byte]

- MCU writes the low-byte of the EEPROM address into I2CDAO register
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CDAO register is transmitted to the device. (EEPROM address)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been sent.

31 Bytes EEPROM [DATA]

- MCU writes the DATA to be written to the EEPROM into I2CDAO register
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CDAO register is transmitted to the device (EEPROM data)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been sent.
- This operation repeats 31 times.

Last Byte EEPROM [DATA]

- MCU sets I2CSTA[SWR] = 1. This forces the I2C controller to generate a stop condition after the content of I2CDAO register is transmitted.
- MCU writes the last DATA byte to be written to the EEPROM into I2CDAO register
- TXE bit in I2CSTA is cleared, indicating busy
- The content of I2CDAO register is transmitted to the EEPROM (EEPROM data)
- TXE bit in I2CSTA is set, and interrupts the MCU, indicating that I2CDAO register has been sent
- I2C controller generates a stop condition after the content of I2CDAO register is transmitted
- END of 32-byte page write operation

3 Electrical Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature (unless otherwise noted)[†]

Supply voltage, V_{CC}	–0.5 V to 4 V
Input voltage, V_I	–0.5 V to V_{CC} + 0.5 V
Output voltage, V_O	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK}	±20 mA
Output clamp current, I_{OK}	±20 mA
Storage temperature	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Commercial Operating Condition

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	High level input voltage	2		V_{CC}	V
V_{IL}	Low level input voltage	0		0.8	V
T_A	Operating temperature	0		70	°C

3.3 Electrical Characteristics, $T_A = 25°C$, $V_{CC} = 3.3 V \pm 0.3V$, GND = 0 V

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.5	V
V_{IT+}	Positive input threshold voltage	$V_I = V_{IH}$			2	V
V_{IT-}	Negative input threshold voltage	$V_I = V_{IH}$	0.8			V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)	$V_I = V_{IH}$		1		V
I_{IH}	High-level input current	$V_I = V_{IH}$			±1	µA
I_{IL}	Low-level input current	$V_I = V_{IL}$			±1	µA
I_{OZ}	Output leakage current (Hi-Z)	$V_I = V_{CC}$ or V_{SS}			10	µA
C_I	Input capacitance			5		pF
C_O	Output capacitance			7		pF
I_{CC}	Quiescent			25	45	mA
I_{CCx}	Suspend			45		µA

4 Application

4.1 Keyboard Section

Table 4–1 outlines the GPIO assignment for the switch-matrix scanning and for keyboard LED drive. Figure 4–1 illustrates the Port-3 pins that are assigned to drive the four keyboard LEDs. As shown, P3[7:4] can sink up to 12 mA (open-drain output). Figure 4–2 illustrates the 18 outputs (open-drain) and the 8 Inputs (internal pullups) that are used for the switch-matrix scanning. Figure 4–3 illustrates the partial connection bus power mode. Figure 4–4 shows the USB upstream connection, and Figure 4–5 illustrates the downstream connection (only one port shown).

Table 4–1. GPIO Assignment for Matrix Scan and LED Drive

GPIO	I/O	
P0[7:0]	O	8–bits Matrix scan outputs
P1[7:0]	O	8–bits Matrix scan outputs
P3.6	O	1–bits Matrix scan outputs
P3.7	O	1–bits Matrix scan outputs
P2[7:0]	I	8–bits Matrix scan Inputs
P3.2	O	Keyboard LED–1
P3.3	O	Keyboard LED–2
P3.4	O	Keyboard LED–3
P3.5	O	Keyboard LED–4
P3.0	I/O	GPIO (Not used for keyboard)
P3.1	I/O	GPIO (Not used for keyboard)

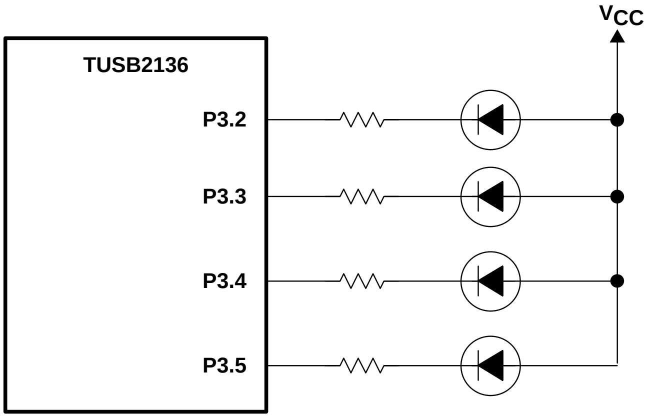


Figure 4–1. Keyboard LED Connection

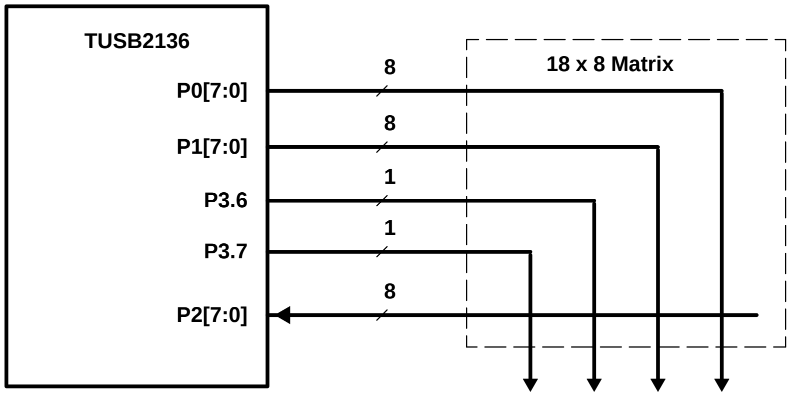


Figure 4–2. Keyboard Matrix Scan Connection

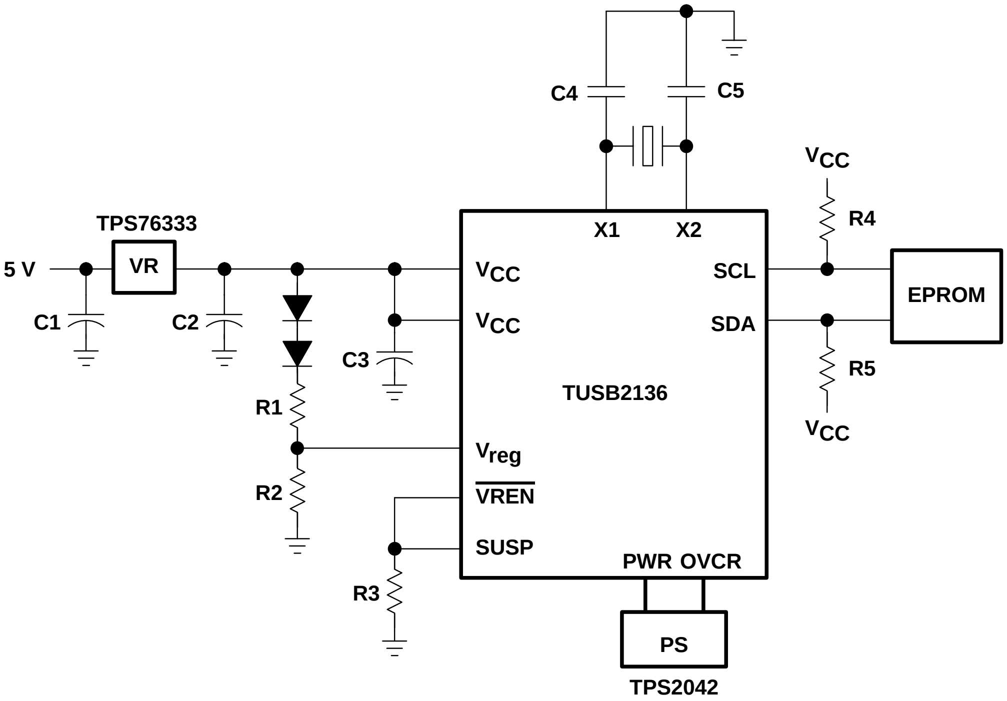


Figure 4–3. Partial Connection Bus Power Mode

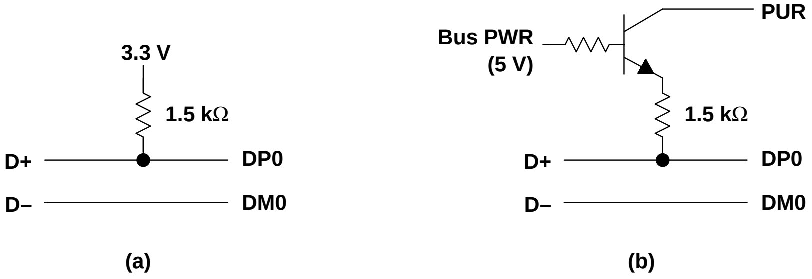


Figure 4–4. Upstream Connection (a) Non-Switching Power Mode (b) Switching Power Mode

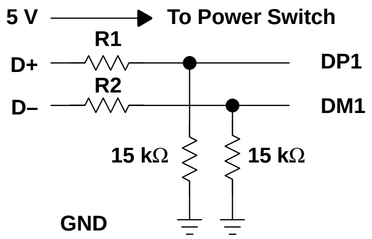


Figure 4–5. Downstream Connection – Only One Port Shown

NOTE: Ferrite beads can be used on power lines to help ESD.

4.2 Reset Timing

There are two requirements for the reset signal timing. First, the reset window should be between 100 µsec and 10 msec. At power up, this time is measured from the time the power ramps up to 90% of the nominal Vcc until the reset signal goes high (above 1.2 V). The second requirement is that the clock has to be valid during the last 60 µsec of the reset window. These two requirements are depicted in Figure 4–6. Notice that when using a 12 MHz crystal or the 48 MHz oscillator, the clock signal may take several milliseconds to ramp up and become valid after power up. Therefore, the reset window may need to be elongated up to 10 msec. to ensure that there is a 60 µsec overlap with a valid clock.

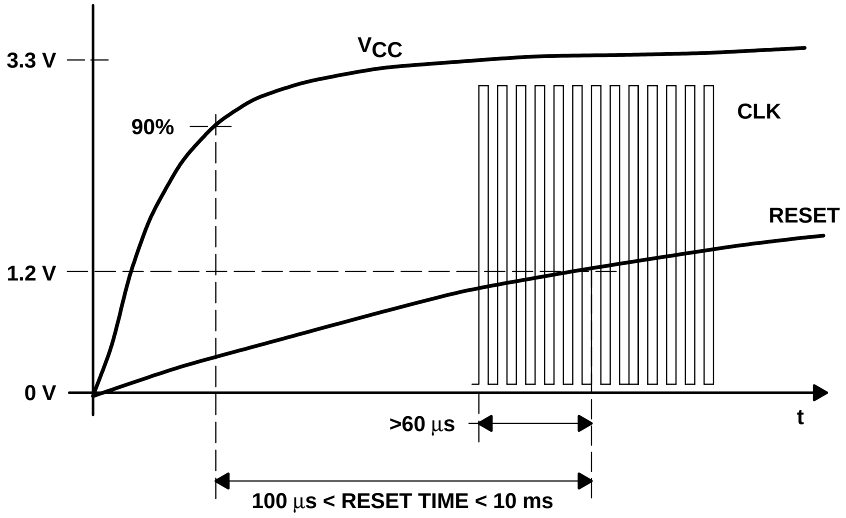
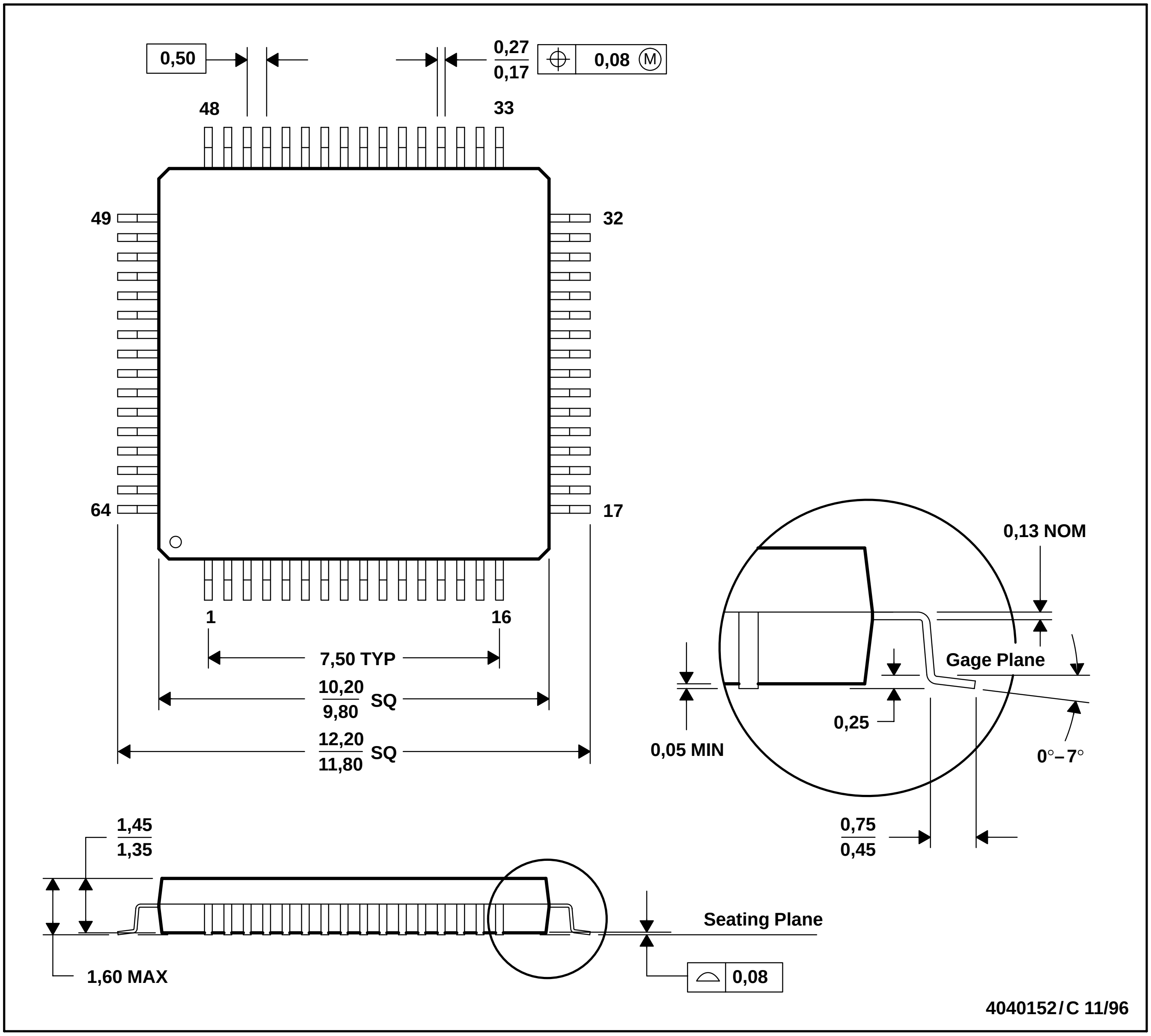


Figure 4–6. Reset Timing

5 Mechanical Data

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026
- D. May also be thermally enhanced plastic with leads connected to the die pads.