winbond

8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W78C051D microcontroller supplies a wider frequency and supply voltage range than most 8-bit microcontrollers on the market. It is compatible with the industry standard 80C51 microcontroller series.

The W78C051D contains four 8-bit bidirectional parallel ports, one extra 4-bit bit-addressable I/O port (Port 4) and two additional external interrupts ($\overline{INT2}$, $\overline{INT3}$), two 16-bit timer/counters, one watchdog timer and a serial port. These peripherals are supported by a seven-source, two-level interrupt capability. There are 128 bytes of RAM and an 4K byte mask ROM for application programs.

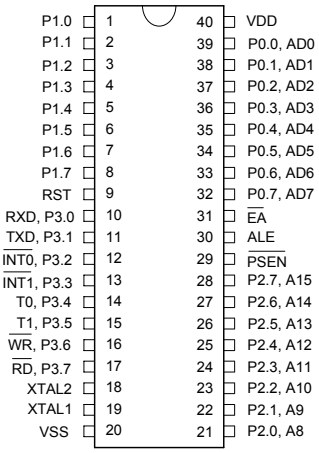
The W78C051D microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

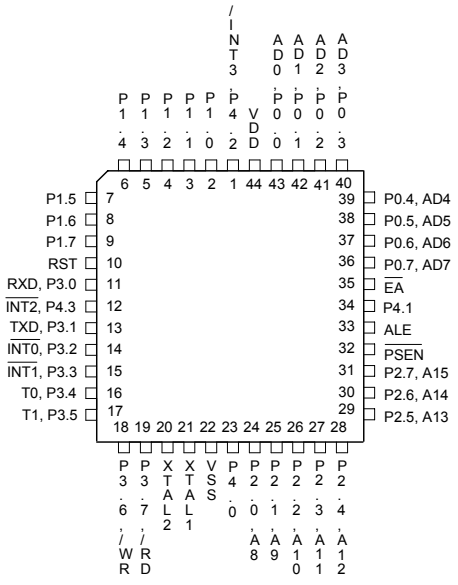
- Fully static design
- Supply voltage of 4.5V to 5.5V
- DC-40 MHz operation
- 128 bytes of on-chip scratchpad RAM
- 4K bytes of on-chip mask ROM
- 64K bytes program memory address space
- 64K bytes data memory address space
- Four 8-bit bidirectional ports
- Two 16-bit timer/counters
- One full duplex serial port
- Seven-source, two-level interrupt capability
- One extra 4-bit bit-addressable I/O port
- Two additional external interrupts $\overline{INT2}$ / $\overline{INT3}$
- Watchdog timer
- EMI reduction mode
- Built-in power management
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78C051D40DL
  - Lead Free (RoHS) PLCC 44: W78C051D40PL
  - Lead Free (RoHS) PQFP 44: W78C051D40FL

3. PIN CONFIGURATIONS

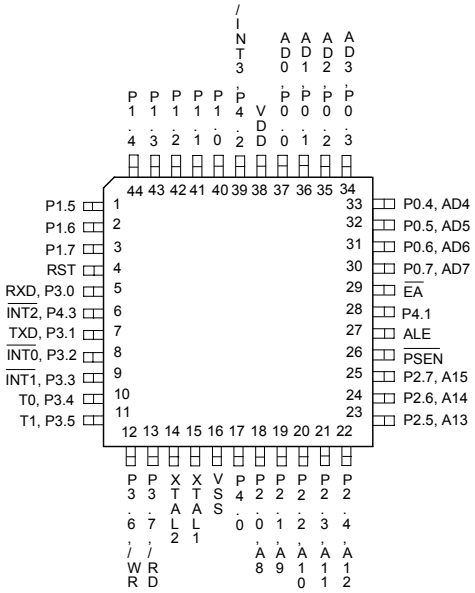
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

P0.0–P0.7

Port 0, Bits 0 through 7. Port 0 is a bidirectional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

P1.0–P1.7

Port 1, Bits 0 through 7. Port 1 is a bidirectional I/O port with internal pull-ups.

P2.0–P2.7

Port 2, Bits 0 through 7. Port 2 is a bidirectional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

P3.0–P3.7

Port 3, Bits 0 through 7. Port 3 is a bidirectional I/O port with internal pull-ups. All bits have alternate functions, which are described below:

PIN	ALTERNATE FUNCTION
P3.0	RXD Serial Receive Data
P3.1	TXD Serial Transmit Data
P3.2	$\overline{\text{INT0}}$ External Interrupt 0
P3.3	$\overline{\text{INT1}}$ External Interrupt 1
P3.4	T0 Timer 0 Input
P3.5	T1 Timer 1 Input
P3.6	$\overline{\text{WR}}$ Data Write Strobe
P3.7	$\overline{\text{RD}}$ Data Read Strobe

P4.0–P4.3

Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{\text{INT2}}$ / $\overline{\text{INT3}}$).

$\overline{\text{EA}}$

External Address Input, active low. This pin forces the processor to execute out of external ROM. This pin should be kept low for all W78C31 operations.

RST

Reset Input, active high. This pin resets the processor. It must be kept high for at least two machine cycles in order to be recognized by the processor.

ALE

Address Latch Enable Output, active high. ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. A single ALE pulse is skipped during external data memory accesses. ALE goes to a high impedance state during reset with a weak pull-up.

$\overline{\text{PSEN}}$

Program Store Enable Output, active low. $\overline{\text{PSEN}}$ enables the external ROM onto the Port 0 address/data bus during fetch and MOVC operations. $\overline{\text{PSEN}}$ goes to a high impedance state during reset with a weak pull-up.

XTAL1

Crystal 1. This is the crystal oscillator input. This pin may be driven by an external clock.

XTAL2

Crystal 2. This is the crystal oscillator output. It is the inversion of XTAL1.

VSS, VDD

Power Supplies. These are the chip ground and positive supplies.

5. FUNCTIONAL DESCRIPTION

The W78C051D architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 128 bytes of RAM, two timer/counters, one watchdog timer and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64 K data storage space.

Timers 0, 1

Timers 0, 1 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1. The TCON and TMOD registers provide control functions for timers 0, 1.

Clock

The W78C051D is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78C051D relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78C051D incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input high level of greater than 3.5 volts when V_{DD} = 5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stopped. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78C051D is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupts $\overline{INT2}$, $\overline{INT3}$ have been added to either the PLCC or QFP package. And description follows:

1. $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

*****XICON - external interrupt control (C0H)**

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Seven-source interrupt information:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
External Interrupt 2	33H	5	XICON.2	XICON.0
External Interrupt 3	3BH	6 (lowest)	XICON.6	XICON.3

2. PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

```
Example:  P4      REG   0D8H
          MOV     P4, #0AH     ; Output data "A" through P4.0–P4.3.
          MOV     A, P4        ; Read P4 status to Accumulator.
          SETB    P4.0         ; Set bit P4.0
          CLR     P4.1         ; Clear bit P4.1
```

Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

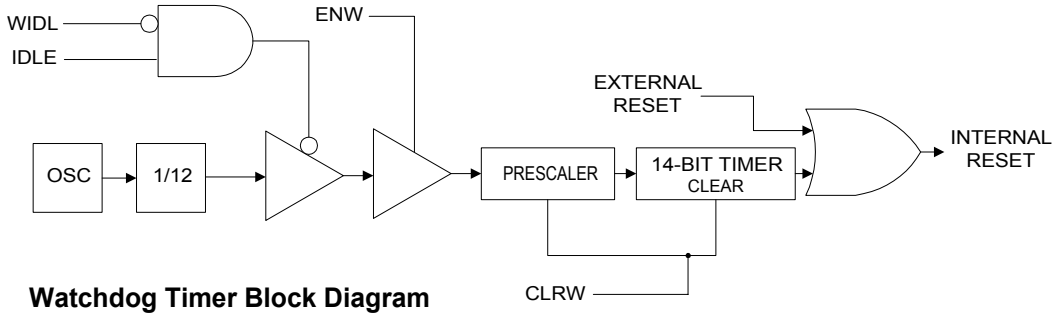
PS2, PS1, PS0 : Watch-dog prescaler timer select. Prescaler is selected when set PS2~0 as follows:

PS2	PS1	PS0	PRESCALER SELECT
0	0	0	2
0	1	0	4
0	0	1	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

The time-out period is obtained using the following formula:

$$\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer , prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watchdog time-out period when OSC = 20 MHz

PS2 PS1 PS0	WATCHDOG TIME-OUT PERIOD
0 0 0	19.66 mS
0 1 0	39.32 mS
0 0 1	78.64 mS
0 1 1	157.28 mS
1 0 0	314.57 mS
1 0 1	629.14 mS
1 1 0	1.25 S
1 1 1	2.50 S

Reduce EMI Emission

Because of the on-chip ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is not needed. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space.

AUXR - Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	AO

Mnemonic: AUXR Address: 8Eh

AO: Turn off ALE signal.

6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{CC}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{CC} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7. DC CHARACTERISTICS

(V_{DD}–V_{SS} = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	20	mA	V_{DD} = 5.5V, 20 MHz, no load
Idle Current	I_{IDLE}	-	6	mA	V_{DD} = 5.5V, 20 MHz, no load
Power Down Current	I_{PWDN}	-	50	μA	V_{DD} = 5.5V, no load
Input Current P1, P2, P3, P4	I_{IN}	-50	+10	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	μA	V_{DD} = 5.5V V_{SS} < V_{IN} < V_{DD}
Input Current RST	I_{IN2}	-10	+300	μA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Logic 1-to-0 Transition Current P1, P2, P3, P4	I_{TL}	-500	-	μA	V_{DD} = 5.5V V_{IN} = 2V
Input					
Input Low Voltage P1, P2, P3, P4	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*4]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
Input High Voltage P1, P2, P3, P4	VIH1	2.4	VDD +0.2	V	VDD = 5.5V
Input High Voltage RST	VIH2	3.5	VDD +0.2	V	VDD = 5.5V
Input High Voltage XTAL1[*4]	VIH3	3.5	VDD +0.2	V	VDD = 5.5V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Output					
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P2, P3, P4	I_{SK1}	4	10	mA	V_{DD} = 4.5V Vin = 0.45V
Sink Current P0, ALE, $\overline{PSEN}$	I_{SK2}	8	16	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Source Current P1, P2, P3, P4	I_{SR1}	-100	-250	μA	V_{DD} = 4.5V V_{IN} = 2.4V
Source Current P0, ALE, $\overline{PSEN}$	I_{SR2}	-8	-14	mA	V_{DD} = 4.5V V_{IN} = 2.4V

Notes:

*1. RST pin has an internal pull-down.

*2. Pins of P1 and P3 can source a transition current when they are being externally driven from 1 to 0.

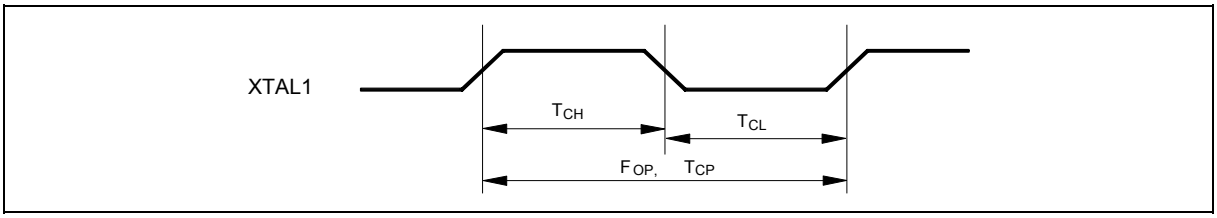
*3. RST is a Schmitt trigger input and XTAL1 is a CMOS input.

*4. P0, P2, ALE and $\overline{PSEN}$ are tested in the external access mode.

8. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.5 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP}-Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP}-Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP}-Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP}-Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP}-Δ	3 T_{CP}	-	nS	4

Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP}-Δ	-	3 T_{CP}+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP}-Δ	6 T_{CP}	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	3 T_{CP}-Δ	-	3 T_{CP}+Δ	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	1 T_{CP}-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	1 T_{CP}-Δ	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	6 T_{CP}-Δ	6 T_{CP}	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

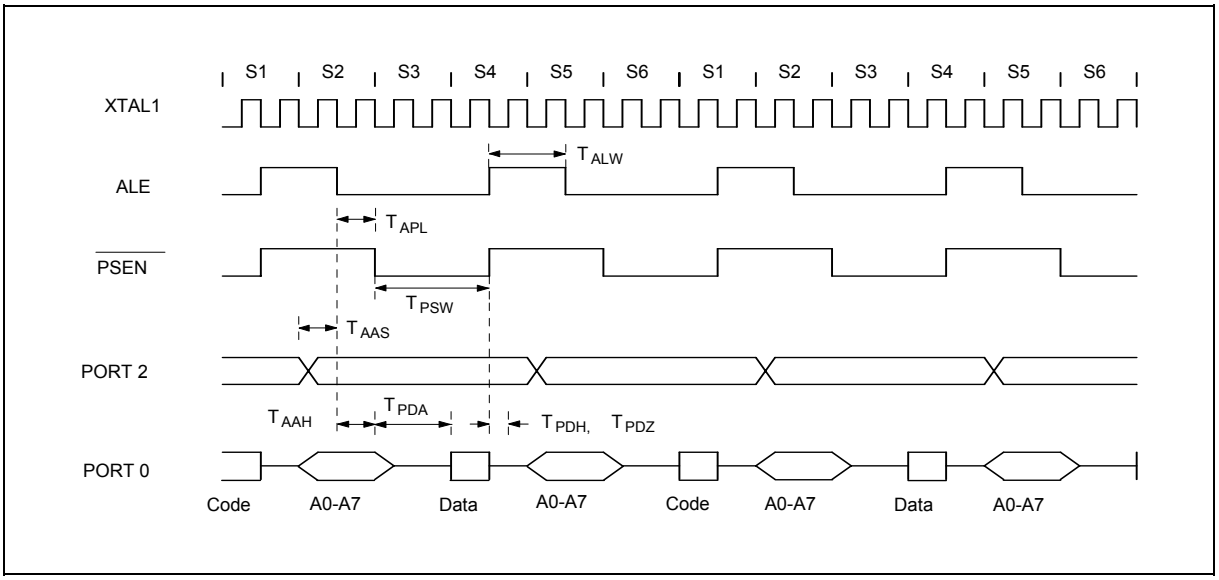
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 T_{CP}	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 T_{CP}	-	-	nS

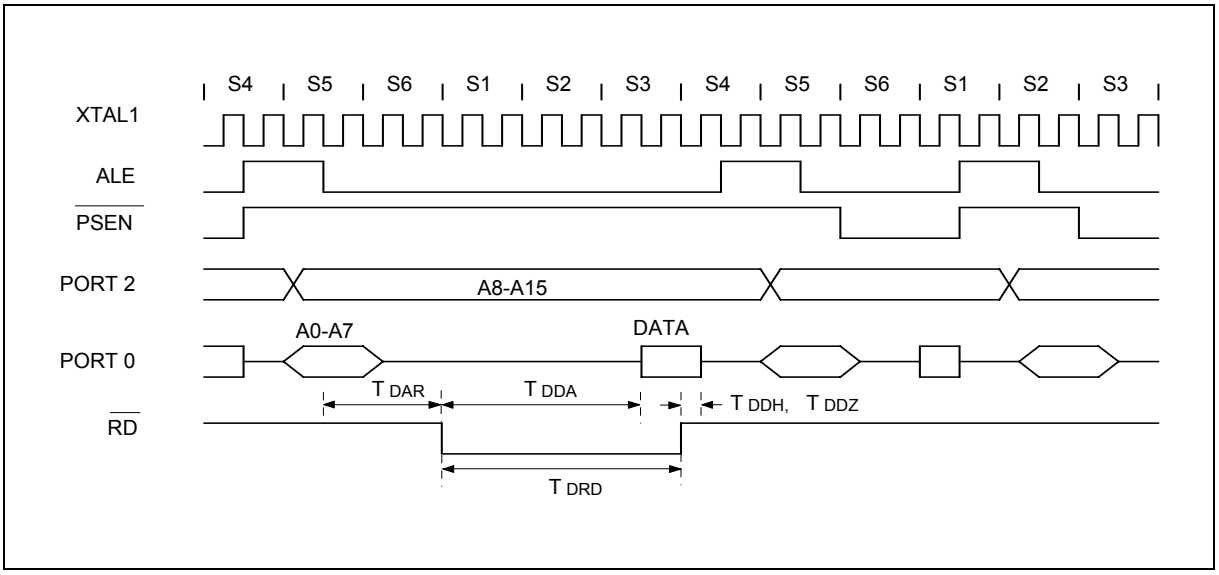
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

9. TIMING WAVEFORMS

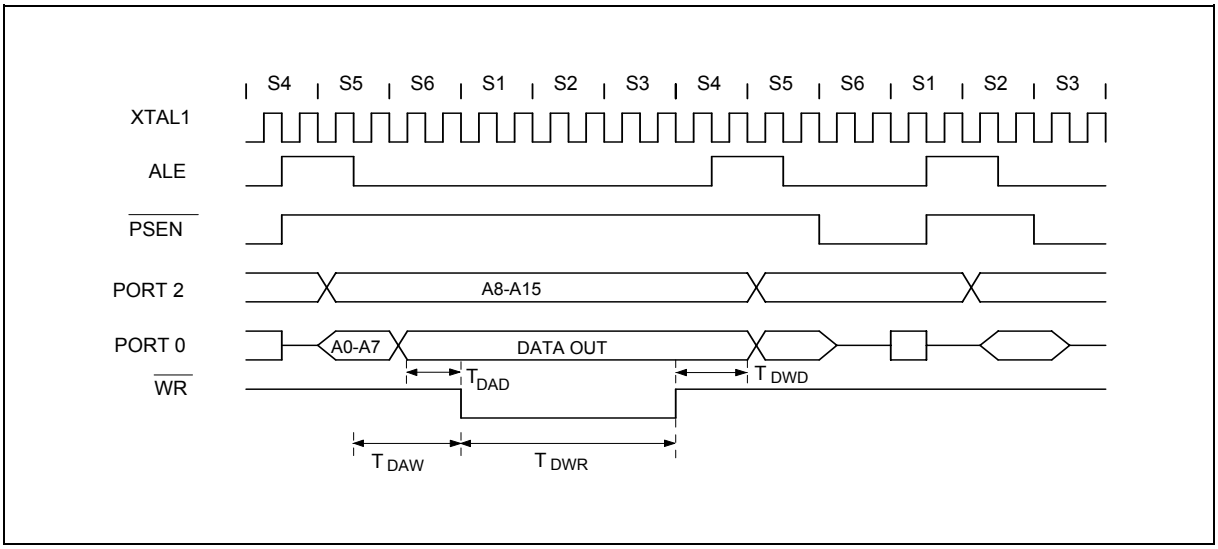
Program Fetch Cycle



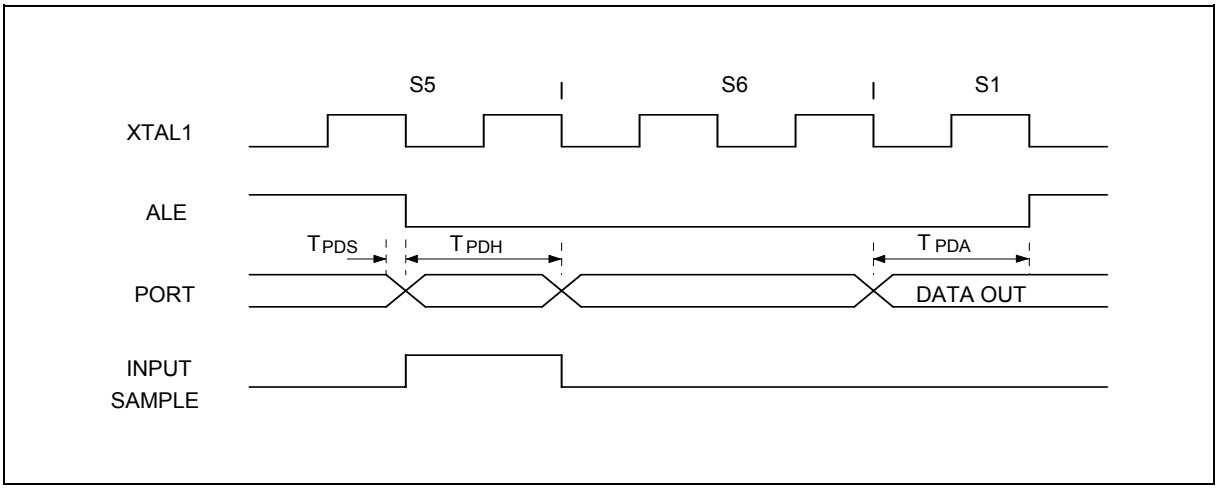
Data Read Cycle



Data Write Cycle



Port Access Cycle



10. APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

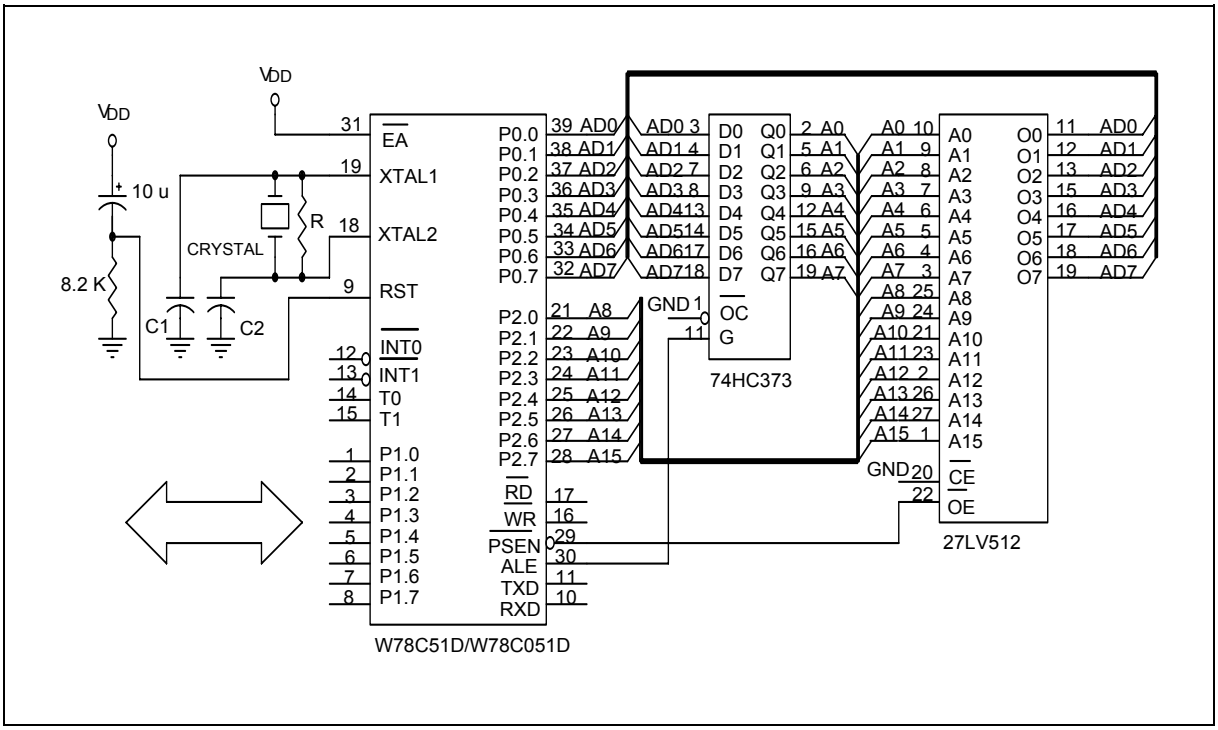


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	_
24 MHz	15P	15P	_
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

Expanded External Data Memory and Oscillator

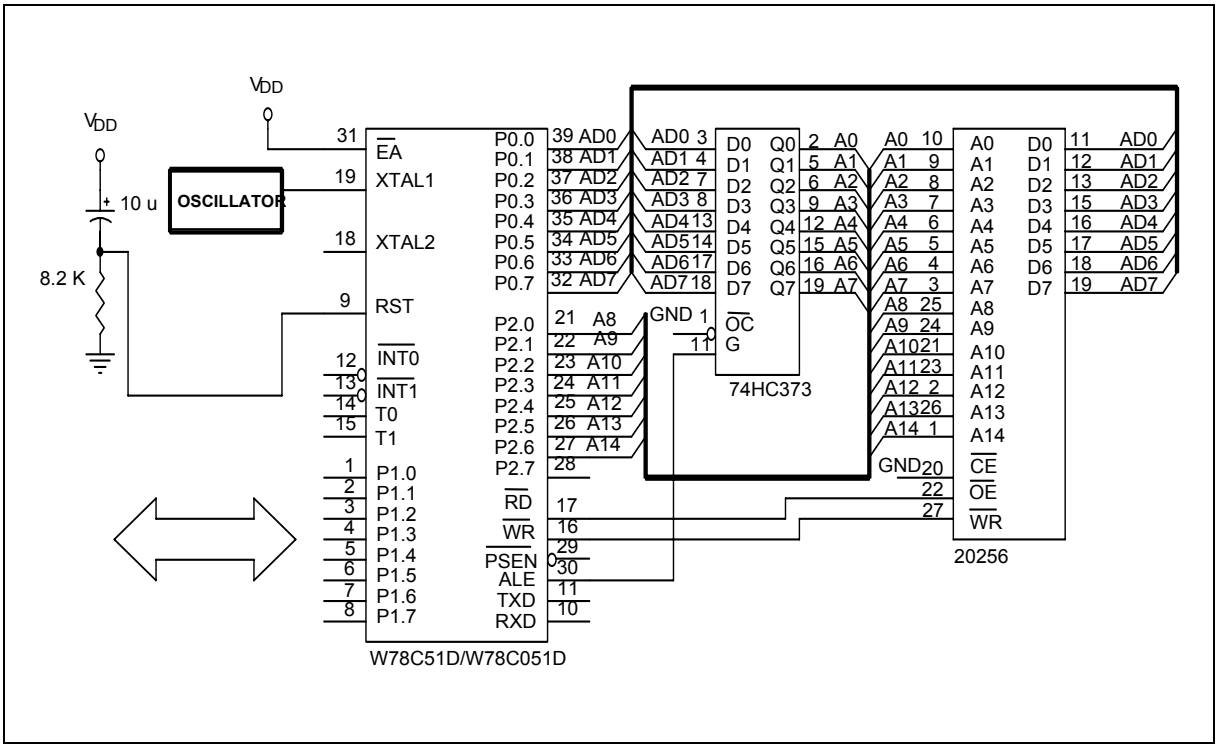
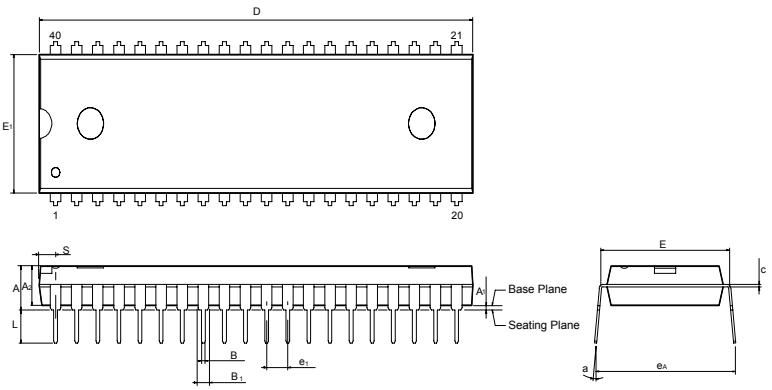


Figure B

11. PACKAGE DIMENSIONS

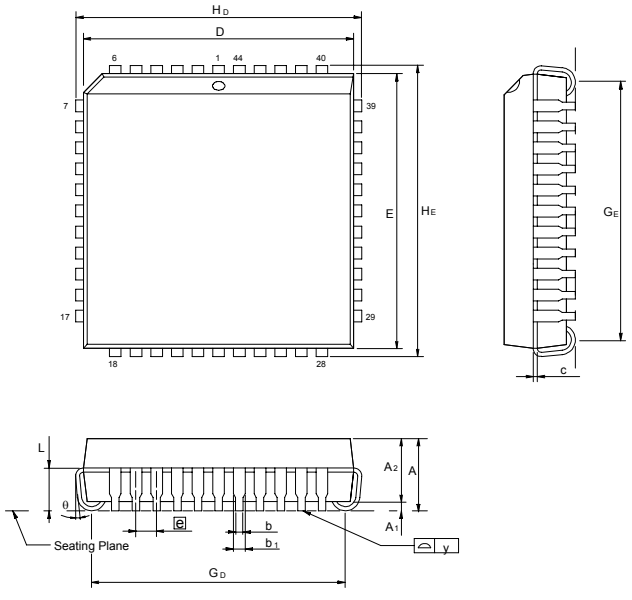
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

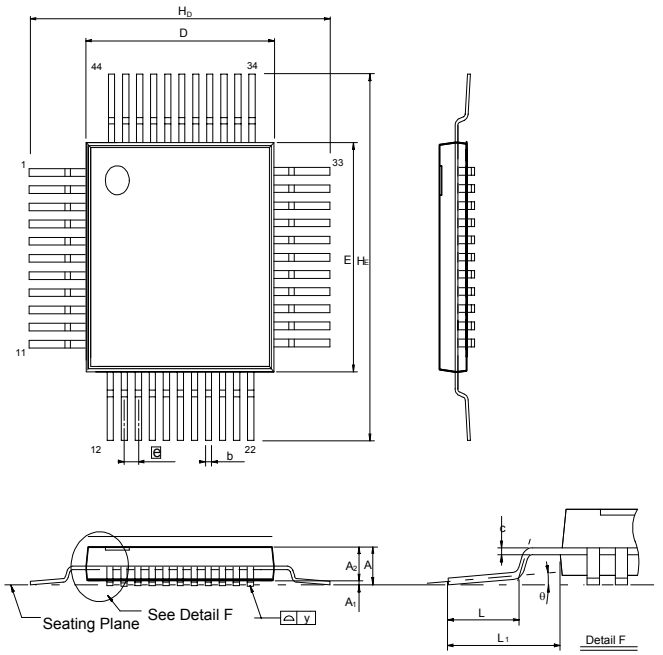
44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	January 1999	-	Initial Issued
A2	April 20, 2005	19	Add Important Notice
A3	December 28, 2005	- 2	Remove “Preliminary” from sheet header Add lead-free(RoHS) parts, Remove 24MHz parts
A4	October 3, 2006		Remove block diagram
A5	December 4, 2006	2	Remove all Leaded package parts
A6	November 20, 2007	7	Remove timer/counter 2 interrupt information

Important Notice

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Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.