



# C8051F061 16-bit ADCs, CAN, 64KB FLASH, 64-Pin MCU

## ANALOG PERIPHERALS

- **Two 16-bit ADC's**
  - Programmable Throughput up to 1Msps (each ADC)
  - $\pm 0.75$  LSB INL; guaranteed no missing codes
  - Configurable as two Single-Ended or one Differential ADC
  - DMA to XRAM
  - Data Dependent Windowed Interrupt Generator
- **10-bit ADC**
  - Programmable Throughput up to 200ksps
  - 8 External Inputs
  - Built-in Temperature Sensor ( $\pm 3^\circ\text{C}$ )
- **Two 12-bit DACs**
  - Can Synchronize Outputs to Timers for Jitter-Free Waveform Generation
- **Three Comparators**
- **Internal Voltage Reference**
- **Precision VDD Monitor/Brown-out Detector**

## ON-CHIP JTAG DEBUG & BOUNDARY SCAN

- On-Chip Debug Circuitry Facilitates Full Speed, Non-Intrusive In-System Debug (No Emulator Required!)
- Provides Breakpoints, Single Stepping, Watchpoints, Stack Monitor
- Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- IEEE1149.1 Compliant Boundary Scan
- Low Cost, **Complete** Development Kit

## 64-Pin TQFP

Temperature Range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

## HIGH SPEED 8051 $\mu\text{C}$ CORE

- Pipelined Instruction Architecture; Executes 70% of Instructions in 1 or 2 System Clocks
- Up to 25MIPS Throughput with 25MHz System Clock
- Expanded Interrupt Handler

## MEMORY

- 4352 Bytes Internal Data RAM (256 + 4k)
- 64k Bytes In-System Programmable FLASH Program Memory

## CAN Bus 2.0B

- 32 Message Objects
- "Mailbox" implementation only interrupts CPU when needed

## DIGITAL PERIPHERALS

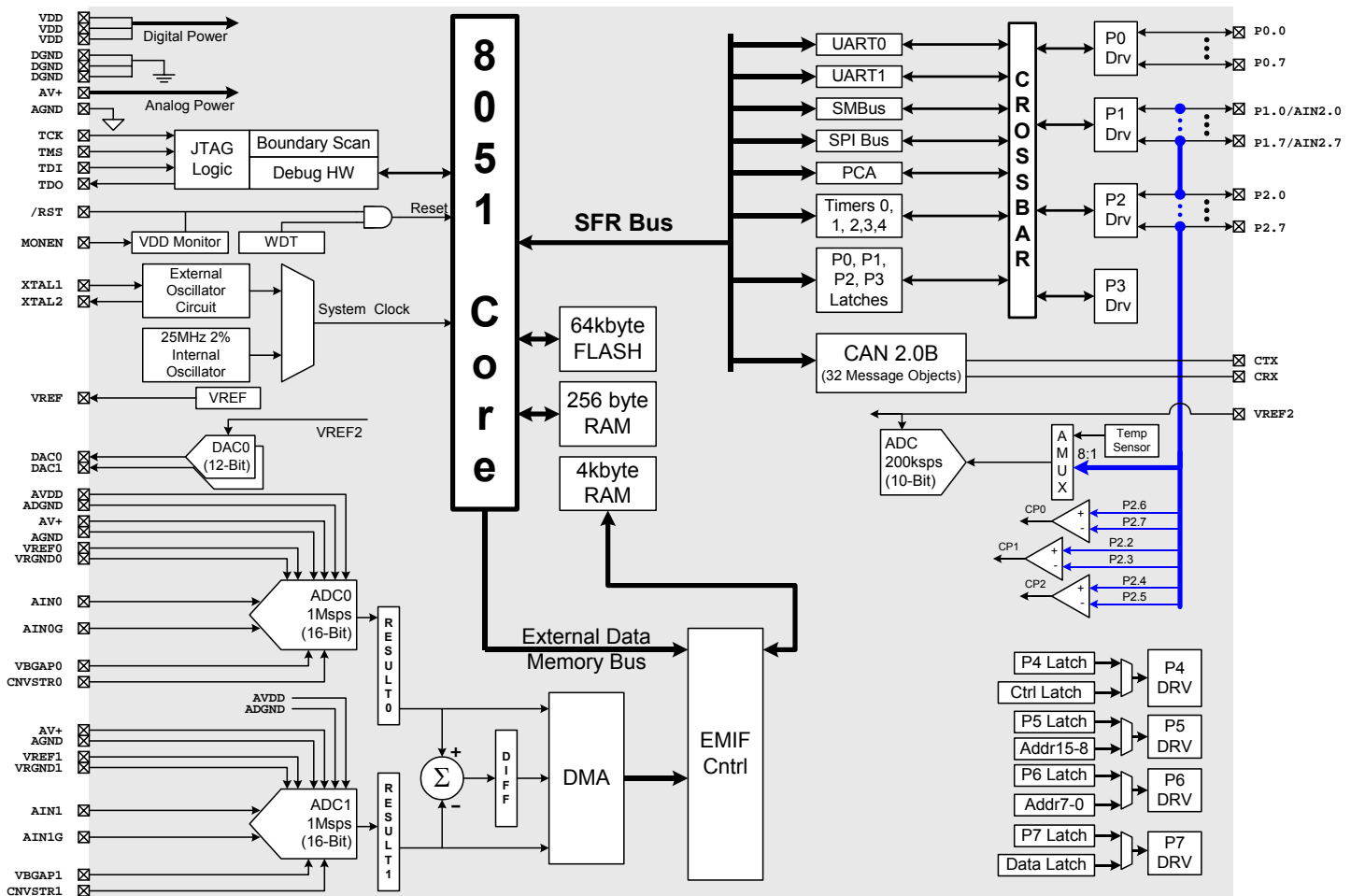
- 24 Port I/O; Port 0 is 5V tolerant
- Hardware SMBus™ (I2C™ Compatible), SPI™, and **Two** UART Serial Ports Available Concurrently
- Programmable 16-bit Counter Array with 6 Capture/Compare Modules
- Five General Purpose 16-bit Counter/Timers
- Dedicated Watch-Dog Timer; Bi-directional Reset

## CLOCK SOURCES

- Internal Programmable 2% Oscillator: 24.5MHz
- External Oscillator: Crystal, RC, C, or Clock
- Real-Time Clock Mode using Timers or PCA

## SUPPLY VOLTAGE ..... 2.7V to 3.6V

- Multiple Power Saving Sleep and Shutdown Modes





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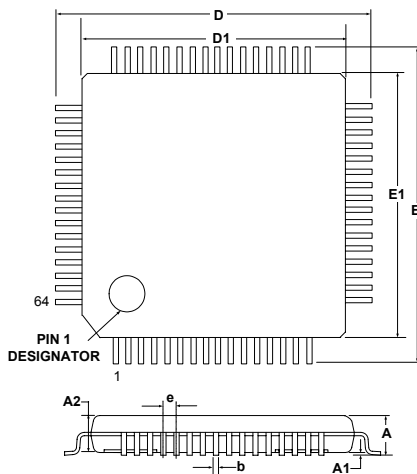
SILICON LABORATORIES

PRELIMINARY

SELECTED ELECTRICAL SPECIFICATIONS  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{V}$  unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GLOBAL CHARACTERISTICS</b>					
Supply Voltage		2.7		3.6	V
Supply Current (CPU active)	Clock=25MHz		18		mA
	Clock=1MHz		0.7		mA
	Clock=32kHz; VDD Monitor Enabled		20		$\mu\text{A}$
Supply Current (shutdown)	Oscillator not running; VDD Monitor Disabled		0.1		$\mu\text{A}$
Clock Frequency Range		DC		25	MHz
<b>16-BIT A/D CONVERTERS</b>					
Resolution			16		bits
Integral Nonlinearity	Single-ended Mode		$\pm 0.75$	$\pm 2$	LSB
	Differential Mode		$\pm 0.50$	$\pm 1$	LSB
Differential Nonlinearity	Guaranteed Monotonic		$\pm 0.5$	$\pm 1$	LSB
Signal-to-Noise Plus Distortion	$F_{in} = 10\text{kHz}$ , Single-ended		86		dB
	$F_{in} = 10\text{kHz}$ , Differential		89		dB
Total Harmonic Distortion	$F_{in} = 10\text{kHz}$ , Single-ended		96		dB
	$F_{in} = 10\text{kHz}$ , Differential		103		dB
Spurious-Free Dynamic Range	$F_{in} = 10\text{kHz}$ , Single-ended		97		dB
	$F_{in} = 10\text{kHz}$ , Differential		104		dB
Throughput Rate				1	Msp/s
Input Voltage Range	Single-ended (AINn – AINnG)	0		VREF	V
	Differential (AIN0-AIN1)	-VREF		VREF	V
Power Supply Current (each ADC)	Operating Mode, 1 Msp/s (AVDD + AV+) Shutdown Mode		5.5		mA
			1		$\mu\text{A}$
<b>D/A CONVERTERS</b>					
Resolution			12		LSB
Differential Nonlinearity				$\pm 1$	LSB
Output Settling Time			10		$\mu\text{s}$

## PACKAGE INFORMATION



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	-	1.05
b	0.17	0.22	0.27
D	-	12.00	-
D1	-	10.00	-
e	-	0.50	-
E	-	12.00	-
E1	-	10.00	-

## C8051F060DK DEVELOPMENT KIT

